RECIPIENT

SPECIFICATIONS

MODEL : **RA-4565SA**

SPEC. No. : **Q15-137-4B**

DATE: **Aug. 28. 2015**

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SPECIFICATION

1. Application

1) This document is applicable to the real time clock module RA-4656SA that are delivered to from Seiko Epson Corp. 2) RoHS compliant

RA-4565SA contains lead in high melting type solder which is exempted in RoHS directive.

3) This Product supplied (and any technical information furnished, if any) by Seiko Epson Corporation shall not be used for the development and manufacture of weapon of mass destruction or for other military purposes. Making available such products and technology to any third party who may use such products or technologies for the said purposes are also prohibited.
4) This product listed here is designed as components or parts for electronics equipment in general consumer use. We do not expect that any of these products would be incorporated or otherwise used as a component or part for the equipment, which requires an systems, and medical equipment, the functional purpose of which is to keep extra high reliability, such as satellite, rocket and other space life.

This RA-4565SA is authorized for Battery Management System for automobile only.

2. Model

The model is RA-4565SA.

3. Packing

It is subject to the packing standard of Seiko Epson Corp.

4. Warranty

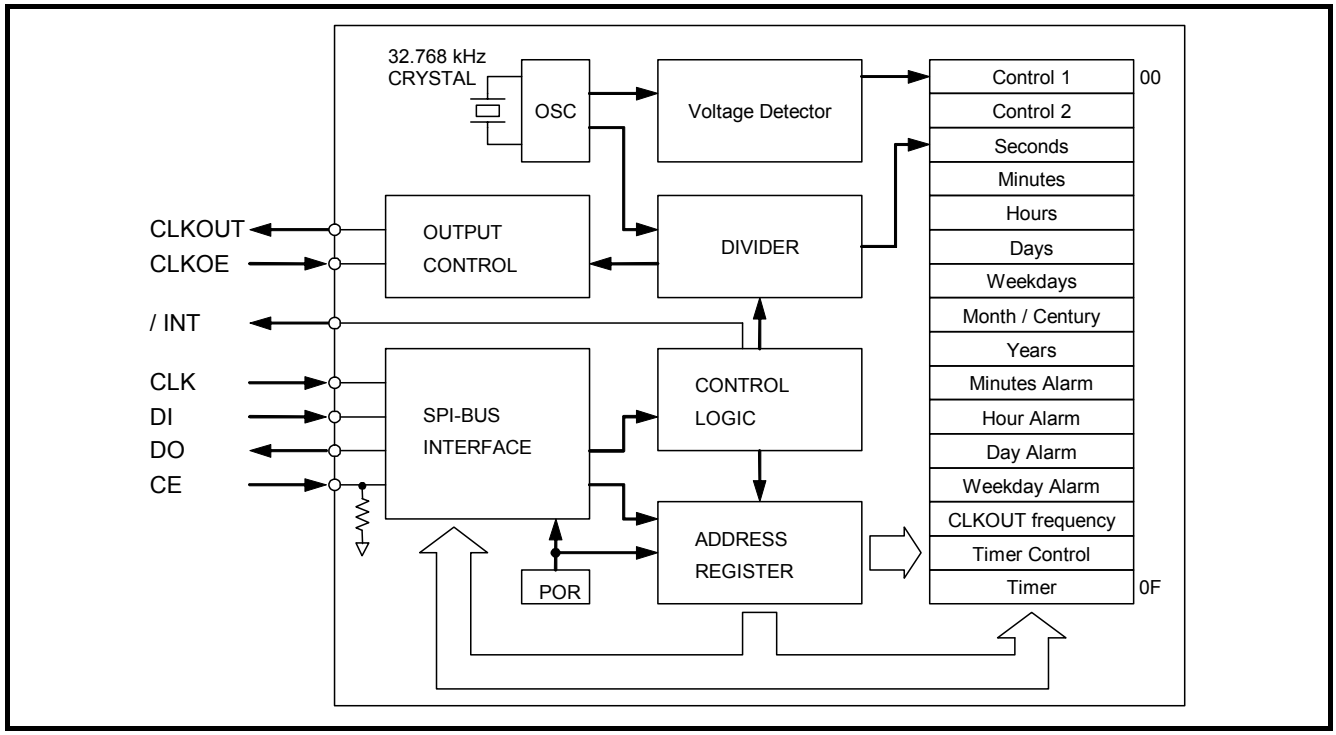
Defective parts which are originated by us are replaced free of charge in case defects are found within 12 Months after delivery.

5. Amendment and abolishment

Amendment and/or abolishment of this specification are subject to the agreement of both parties.

6. Contents

1. Block Diagram



2.Register table

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
00	Control 1	TEST	×	STOP	×	TEST	×	×	×	∗3 , ∗4
01	Control 2	×	×	×	TI / TP	AF	TF	AIE	TIE	∗4
02	Seconds	VL	40	20	10	8	4	2	1	∗1
03	Minutes	×	40	20	10	8	4	2	1	∗4
04	Hours	×	×	20	10	8	4	2	1	∗4
05	Days	×	×	20	10	8	4	2	1	∗4
06	Weekdays	×	×	×	×	×	4	2	1	∗4
07	Months	×	×	×	10	8	4	2	1	∗4
08	Years	80	40	20	10	8	4	2	1	
09	Minute Alarm	AE	40	20	10	8	4	2	1	
0A	Hour Alarm	AE	×	20	10	8	4	2	1	∗4
0B	Day Alarm	AE	×	20	10	8	4	2	1	∗4
0C	Weekday Alarm	AE	×	×	×	×	4	2	1	∗4
0D	CLKOUT frequency	×	×	×	×	×	×	FD1	FD0	∗2 , ∗4
0E	Timer control	TE	×	×	×	×	×	TD1	TD0	∗4
0F	Timer	128	64	32	16	8	4	2	1	

Note) During the initial power-on (from 0 V) and if the value of the VL bit is "1" when the VL bit is read, be sure to initialize all registers before using them.
When doing this, be careful to avoid setting incorrect data as the date or time, as timed operations cannot be guaranteed if incorrect date or time data has been set.

∗1. During the initial power-on (from 0 V), the power-on reset function sets "1" to the VL bit.
∗ Since the value of other registers is undefined at this time, be sure to reset all registers before using them.

∗2. During the initial power-on (from 0 V), the power-on reset function resets the FD1 and FD0 bits to "0".
∗ If the CLKOE input pin is at high level ("H"), output from the CLKOUT output pin is at 32.768(kHz.

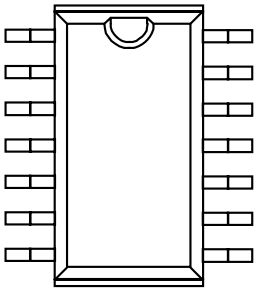
∗3. The two TEST bits for address 00 (Control(1)(are for use by Epson Toyocom Corporation.
When initializing, be sure to write "0". Afterward, be sure to write "0" whenever writing to these bits.
(This device's operations are not guaranteed if "1"(has been set to any of these bits.

∗4. The ' × ' mark indicates when "0" should be set.
The ' × ' mark is undefined when read. This bit should be masked after being read.

3. Terminal description

3.1. Terminal connections

RA – 4565 SA



1. CLK	14. V_{DD}
2. DI	13. CLKOUT
3. DO	12. CLKOE
4. CE	11. N.C.
5. /INT	10. N.C.
6. N.C.	9. N.C.
7. GND	8. N.C.

SOP – 14pin

3.2. Pin Functions

<table>
<tr><th>Signal name</th><th>I/O</th><th>Function</th></tr>
<tr><td>CE</td><td>Input</td><td>This is the chip enabled input pin. It has a built-in pull-down resistance.
When CE pin is at the "H" level, access to this RTC becomes possible.</td></tr>
<tr><td>CLK</td><td>Input</td><td>This is the shift clock input pin for serial data transfer.
In the write mode, it takes in data from the DI pin using the CLK signal rise edge. In the read mode, it outputs data from the DO pin using the fall edge.</td></tr>
<tr><td>D I</td><td>Input</td><td>This is the data input pin for serial data transfer.</td></tr>
<tr><td>DO</td><td>Output</td><td>This is the data output pin for serial data transfer.
∗ When access, please give pull-up treatment to DO pin with high resistance.</td></tr>
<tr><td>CLKOUT</td><td>Output</td><td rowspan="2">The CLKOUT pin is a clock output (open drain output) pin with control output.
The CLKOE pin is an input pin used to control the output mode of the CLKOUT output pin.
The CLKOE input pin can be used in combination with the FD1 bit and FD0 bit to select the output frequency from the CLKOUT output pin (32.768 kHz, 1024 Hz, 32 Hz, or 1 Hz) or to stop output. When output is stopped, the CLKOUT output pin is at high impedance.
<table>
<tr><th>CLKOE pin input</th><th>FD1 bit</th><th>FD0 bit</th><th>CLKOUT pin output</th></tr>
<tr><td rowspan="4">" H "</td><td>0</td><td>0</td><td>32768 Hz Output (open-drain output)</td></tr>
<tr><td>0</td><td>1</td><td>1024 Hz Output (open-drain output)</td></tr>
<tr><td>1</td><td>0</td><td>32 Hz Output (open-drain output)</td></tr>
<tr><td>1</td><td>1</td><td>1 Hz Output (open-drain output)</td></tr>
<tr><td>" L "</td><td>X</td><td>X</td><td>OFF (high impedance)</td></tr>
</table>
During the initial power-on (when power is applied from 0 V), if the CLKOE input pin is at high level (= H), the power-on reset function selects 32.768 kHz as the frequency.</td></tr>
<tr><td>CLKOE</td><td>Input</td></tr>
<tr><td>/INT</td><td>Output</td><td>This pin outputs alarm signals, fixed timer interrupt signals, and other interrupt signals at low level (= " L "). This pin is an open drain pin.</td></tr>
<tr><td>V_{DD}</td><td>–</td><td>This pin connects to the plus side of the power.</td></tr>
<tr><td>GND</td><td>–</td><td>This pin connects to the minus side (ground) of the power.</td></tr>
<tr><td>N.C.</td><td>–</td><td>This pin is not connected internally. Be sure to connect using OPEN, or GND or V_{DD}.</td></tr>
</table>

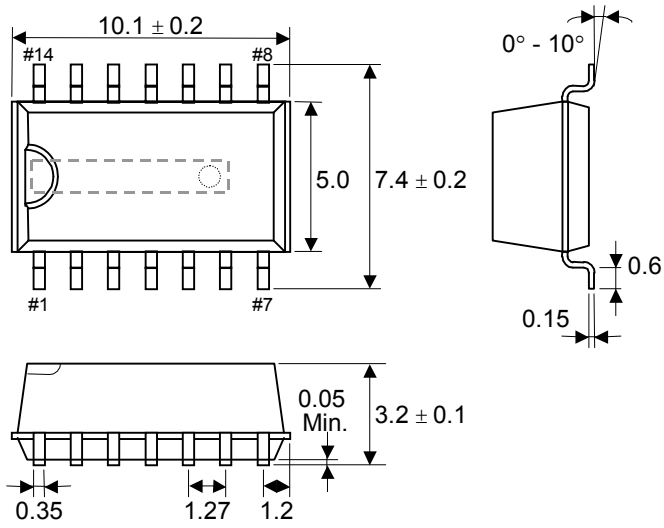
Note : Be sure to connect a bypass capacitor rated at least 0.1 μF between V_{DD} and GND.

4. Dimensions / Marking Layout

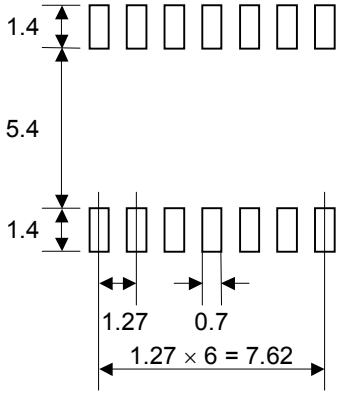
4.1. External dimensions

RA - 4565 SA (SOP-14pin)

• External dimensions



• Recommended soldering pattern

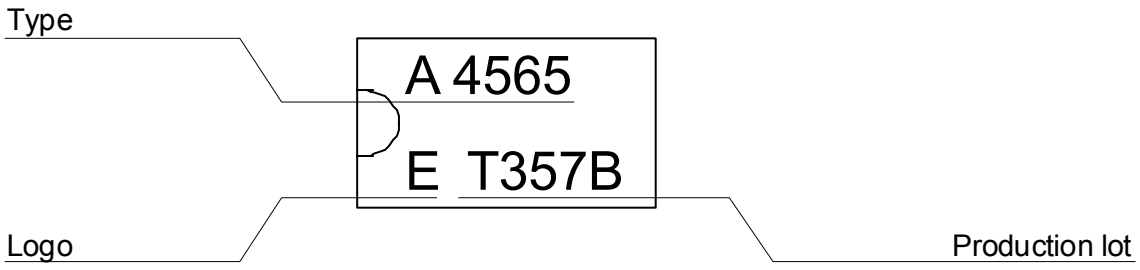


Unit : mm

∗ The cylinder of the crystal unit can be seen in this area (front), but it has no affect on the performance of the device.

4.2. Marking layout

RA - 4565 SA (SOP-14pin)



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

5. Absolute Maximum Ratings

GND = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Between V_{DD} and GND	−0.5 to +6.5	V
Supply Voltage	I_{DD}	V_{DD} pin	−50 to 50	mA
Input Voltage	V_I	CE, CLK, DI pins	GND−0.5 ~ +6.5	V
		CLKOE pin	GND−0.5 ~ V_{DD}+0.5	V
Output Voltage	V_O	CLKOUT, /INT pins	GND−0.5 ~ 6.5	V
		DO pin	GND−0.5 ~ V_{DD}+0.5	V
DC Input Current	I_I		−10 to 10	mA
DC Output Current	I_O		−10 to 10	mA
Storage Temperature Range	T_{STG}	Stored bare product after unpacking	−55 to +125	°C

6. Recommended operating conditions

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Operating supply voltage	V_{DD}		1.6 to 5.5	V
Clock supply voltage	V_{CLK}		1.5 to 5.5	V
Operating temperature	T_{OPR}	No condensation	−40 to +125	°C

7. Frequency Characteristics

* Unless otherwise specified, GND = 0 V , V_{DD} = 3.0 V , Ta = +25 °C

Item	Symbol	Comments		Min.	Typ.	Max.	Unit
Output frequency	fo				32.768 (Typ.)		kHz
Frequency precision	Δ f / f	Ta = +25 °C V_{DD} = 3.0 V			B : 5 ± 23 (*1)		× 10^{-6}
Frequency voltage characteristics	f / V	Ta = +25 °C V_{DD} = 2.0 V to 5.5 V			± 2 (Max.)		× 10^{-6} / V
Frequency temperature characteristics	Top	V_{DD} = 3.0 V Reference at +25 °C	Ta = −40 °C to +125 °C	−600		+10	× 10^{-6}
			Ta = −40 °C to +85 °C	−240		+10	× 10^{-6}
			Ta = −20 °C to +70 °C	−120		+10	× 10^{-6}
Oscillation startup-up time	t_{STA}	V_{DD} = 1.6 V	Ta = −40 °C ~ +125 °C			3.0	s
			Ta = +25 °C		0.5	1.5	s
Aging	fa	Ta = +25 °C , V_{DD} = 3.0 V ; first year		−5		+5	× 10^{-6} / year

*1) This difference is 1 minute by 1 month. (excluding offset)

8. Electrical Characteristics

8.1. DC characteristics

8.1.1. DC characteristics (1)

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +125 °C

Item	Symbol		Condition	Min.	Typ.	Max.	Unit
Current consumption ∗ interface inactive (f_{CLK} = 0 Hz) ∗ CLKOUT = disabled (CLKOE = GND)	I_{DD}	V_{DD} = 5.0 V	Ta = +125 °C		1.0	2.0	μA
			Ta = –40 °C to +85 °C		0.6	1.2	
		V_{DD} = 3.0 V	Ta = +125 °C		0.8	1.6	
			Ta = –40 °C to +85 °C		0.5	1.0	
		V_{DD} = 2.0 V	Ta = +125 °C		0.8	1.5	
			Ta = –40 °C to +85 °C		0.5	0.9	
Current consumption ∗ interface inactive (f_{CLK} = 0 Hz) ∗ CLKOUT = 32 kHz output (CLKOE = V_{DD})	I_{DD32K}	V_{DD} = 5.0 V	Ta = +125 °C		1.5	4.0	μA
			Ta = –40 °C to +85 °C		1.1	2.2	
		V_{DD} = 3.0 V	Ta = +125 °C		1.1	2.2	
			Ta = –40 °C to +85 °C		0.7	1.4	
		V_{DD} = 2.0 V	Ta = +125 °C		0.9	1.8	
			Ta = –40 °C to +85 °C		0.6	1.2	
"L" output current	I_{OL} (DO)		V_{OL} = 0.4 V, V_{DD} = 5 V	–1.5			mA
	I_{OL} (/INT)		V_{OL} = 0.4 V, V_{DD} = 5 V	–2			
	I_{OL} (CLKOUT)		V_{OL} = 0.4 V, V_{DD} = 5 V	–2			
	I_{OL} (DO)		V_{OL} = 0.4 V, V_{DD} = 3 V	–1			
	I_{OL} (/INT)		V_{OL} = 0.4 V, V_{DD} = 3 V	–1			
	I_{OL} (CLKOUT)		V_{OL} = 0.4 V, V_{DD} = 3 V	–1			
Leakage current	I_{LO}		V_O = V_{DD} or GND	–1	0	1	μA

8.1.2. DC characteristics (2)

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +125 °C

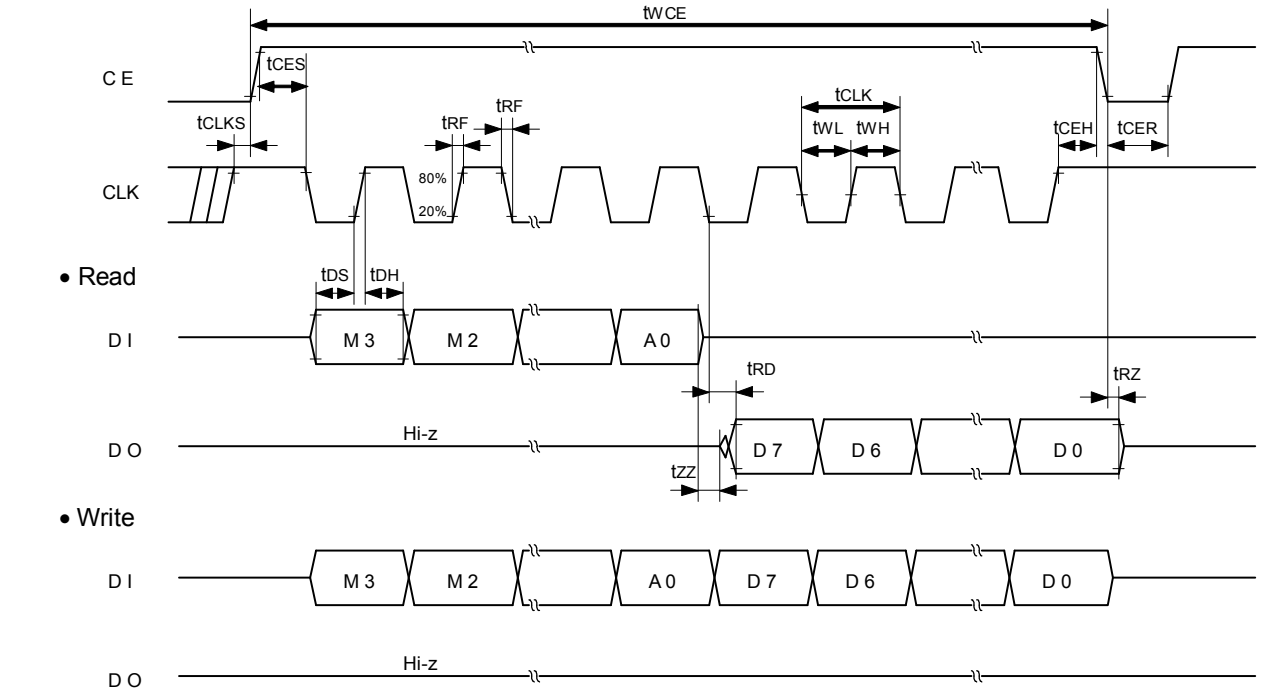
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"L" input voltage	V_{IL}		GND – 0.3		0.3 × V_{DD}	V
"H" input voltage	V_{IH} (CE, CLK, DI)		0.7 × V_{DD}		6.5	V
	V_{IH} (CLKOE)		0.7 × V_{DD}		V_{DD} + 0.5	V
Input resistance	R_{DWN} (CE)			240	550	kΩ

8.2. AC electrical characteristics

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +125 °C

Parameter	Symbol	V_{DD} = 1.6 V < 2.7 V		V_{DD} = 3 V ± 10 %		V_{DD} = 5 V ± 10 %		V_{DD} = 5.5 V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CLK clock frequency	f_{CLK}		2.00		3.33		4.34		4.76	MHz
clock cycle CLK	t_{CLK}	500		300		230		210		ns
CLK pulse width high	t_{WH}	180		130		120		110		ns
CLK pulse width low	t_{WL}	320		170		110		100		ns
CLK rise and fall time	t_{RF}		100		100		100		100	ns
CLK setup time	t_{CLKS}	0		0		0		0		ns
CE setup time	t_{CES}	50		50		50		50		ns
CE hold time	t_{CEH}	70		40		40		30		ns
CE recovery time	t_{CER}	50		50		50		50		ns
Pulse width CE	t_{WCE}		0.99		0.99		0.99		0.99	s
DI setup time	t_{DS}	30		30		30		30		ns
DI hold time	t_{DH}	100		60		40		40		ns
DO read dely time ∗1	t_{RD}		320		170		120		110	ns
DO disable time ∗2	t_{RZ}		50		30		30		25	ns
Bus conflict avoidance time	t_{ZZ}	0		0		0		0		ns

Timing chart



Note: Please make finish one access to this device within 0.95 second (Refer to tWCE).
If more than 1 seconds is taken, time correction may not be done properly.

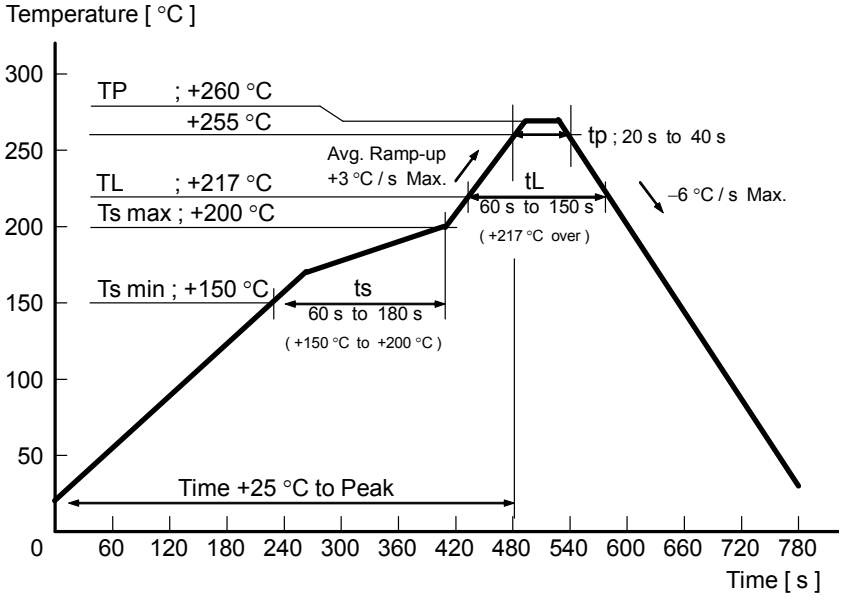
9. Environmental and mechanical characteristics

(The company evaluation condition We evaluate it by the following examination item and examination condition.)

No.	Item	Value *1		Test Conditions
		$\Delta f / f$ [1×10^{-6}] *2	Electrical characteristics	
1	High temperature storage	*3 ± 20	Satisfy item 【5】after test (Includes frequency characteristics)	+125 °C × 1 000 h
2	Low temperature storage	*3 ± 20		-55 °C × 1 000 h
3	High temperature bias	*3 ± 20		+125 °C × 5.5 V × 1 000 h
4	Low temperature bias	*3 ± 20		-40 °C × 5.5 V × 1 000 h
5	Temperature humidity bias	*3 ± 20		+85 °C × 85 %RH × 5.5 V × 1 000 h
6	Temperature cycle	*3 ± 10		-40 °C ⇔ +125 °C 30 min at each temp. 1 000 cycles
7	Resistance to soldering heat	± 8		For convention reflow soldering furnace (3 times) JEDEC J-STD-020C
8	Drop	± 5		Free drop from 750 mm height on a hard wooden board for 3 times (Board is thickness more than 30 mm)
9	Vibration	± 5		10 Hz to 55 Hz amplitude 0.75 mm 55 Hz to 500 Hz acceleration 98 m/s^2 10 Hz → 500 Hz → 10 Hz 15min./cycle 6 h (2 hours , 3 directions)
10	Solderability	Termination must be 95 % covered with fresh solder		Dip termination into solder bath at +235 °C ± 5 °C for 5 s (Using Rosin Flux)

1. *1 Each test done independently.
2. *2 Measuring 2 h to 24 h later leaving in room temperature after each test.
3. *3 Pre conditionings
   1. +125 °C × 24 h to +85 °C × 85 % × 168 h → reflow 3 times
   2. Initial value shall be after 24 h at room temperature.
4. *4 After each Test,satisfy item 7.Frequency characteristics(exclude Aging) and item 8.Electrical Characteristics.

♦ Air-reflow (JEDEC J-STD-020C)



10. Matters that demand special attention on use

10.1. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup

- The RA-4565 SA does not allow access (read or write) when there is no internal oscillation (= stopped oscillation).
  Therefore, we recommend that the first access during power-on initialization or backup and restore operations (i.e., when the power supply voltage is recovered after oscillation has stopped due to a voltage drop, etc.) should be performed after starting internal oscillation and waiting for the oscillation stabilization time (see tSTA standard) to elapse.

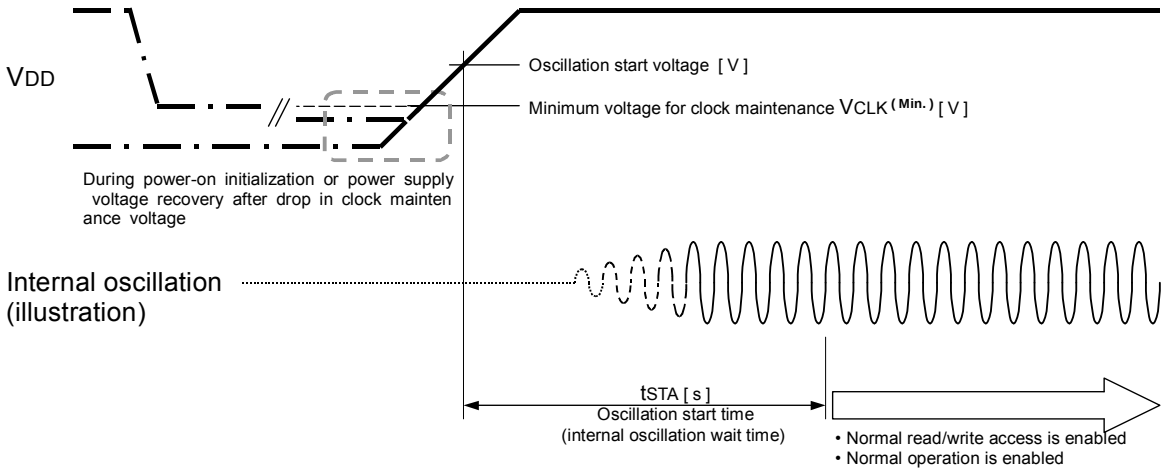
- Note the following caution points concerning access operations during power-on initialization or when restoring the power supply voltage from backup mode (hereafter referred to as "switching to the operating voltage").

  1) Before switching to the operating voltage, read the VL-bit (which indicates the RTC error status).

  2) Initialization is required when the value read from the VL-bit is "VL = 1 (error status)".
  Initialize after the oscillation stabilization time has elapsed.

Initialization is required when the status after reading a VL-bit value of "1" is any of the following. (Status 1) During power-on initialization (Status 2) When only "VL = 1" can be read since internal oscillation is stopped and normal access is disabled (Status 3) When normal access is enabled but the clock setting is invalid due to a voltage drop during backup, etc.

  ∗ Access timing during power-on initialization and when recovering the power supply voltage after a drop in the voltage used to maintain the clock



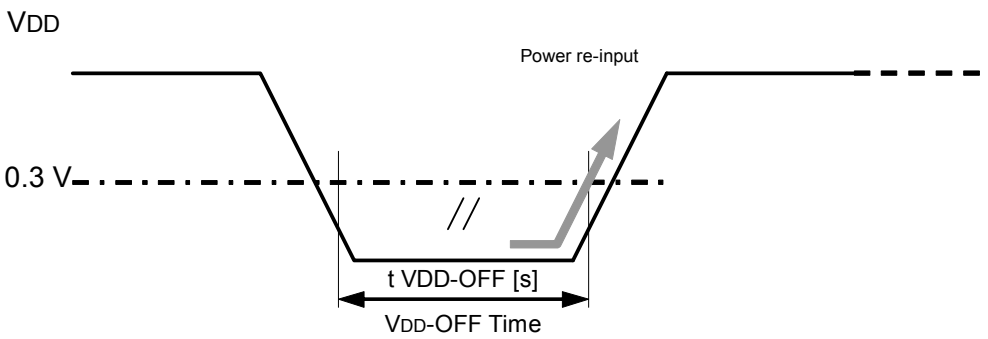
  3) When the read VL-bit value is "VL = 0 (normal status)", access is enabled without waiting for stabilization of oscillation.

Normal operation is enabled under the following two statuses when "0" is read as the VL-bit value. (Status 1) When correct operation is enabled (except for settings errors while in use) (Status 2) When data is retained normally while switching to the operating voltage from backup mode

Note)
When access, please give pull-up treatment to DO pin with high resistance.
* If read out when input initial power and when 「Without internal oscillation = Stop oscillation」 for example back up recovery error, misjudgment that has no pull up resistance on DO pin (originally it should be VL-bit = “1”) and misreading with VL-bit of “0” may be happened.

10.2 Notes to make movement of power-on reset function when re-input power.

Please secure power OFF time (tVDD-OFF [s]) to make movement of power-on reset function.



Before power re-input, please surely keep OFF time tVDD-OFF[s] of VDD which can get [VDD ≤ 0.3 V] for 5 seconds。

[If there is already power OFF time more than 5 seconds] for example when input initial power etc. the above-mentioned time is no needed.

10.3 Notes when use CLKOUT output function and fixed cycle timer interrupting function.

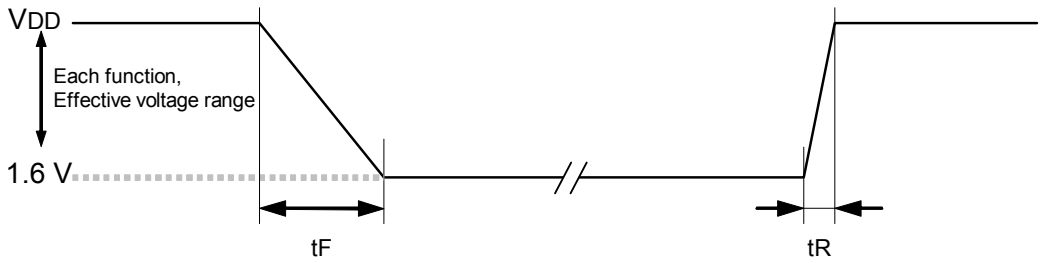
Notes 1) Power voltage range with effective CLKOUT output function and fixed cycle timer interrupt function.

Power voltage range with effective CLKOUT output function and fixed cycle timer interrupt function is 1.6 V to 5.5 V. (Please refer to movement power voltage rule)

Notes 2) Power voltage change under the condition of using CLKOUT output function and fixed cycle timer interrupt output function.

If power voltage is largely changed, each output may be stopped for several ms due to such change. If it is also necessary to keep each output condition when change power voltage, please make consideration to get slow change of power.

If change power voltage during output of each function
(Soon after switching over to backup, or soon after returning from backup etc.), please make consideration the followings.



If it is necessary to keep each output condition, please make consideration to get slow power decreasing with over 10ms/V.

If it is necessary to keep each output condition, please make consideration to get slow power increasing with over 1ms/V.

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

(5) This product is qualified at JEDEC J-STD -020C Moisture Sensitive Level 1.

After open the packing, we recommend to keep it less than +30 °C and 85 %RH of Humidity,and use it less than 6 months.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

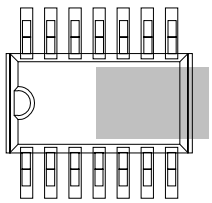
(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

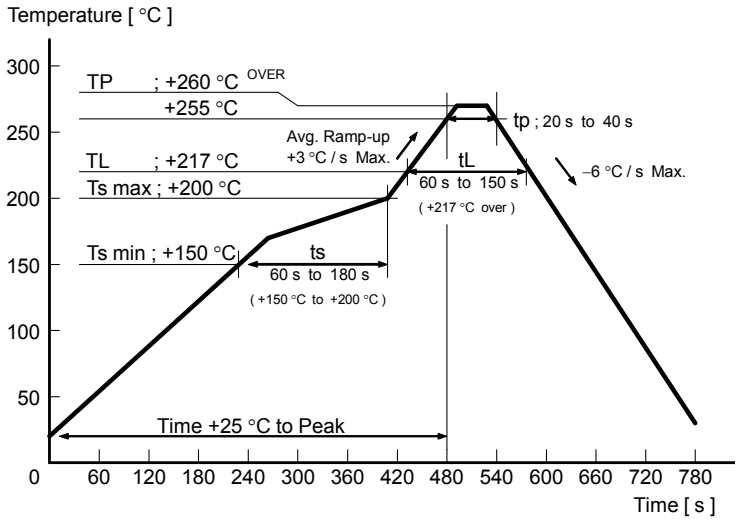
RA – 4565 SA

(SOP – 14 pin)



* The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



TAPING SPECIFICATION

Ⅰ. Application

This standard will apply to SOP 14 pin package.

Spec：SA package

Ⅱ. Contents

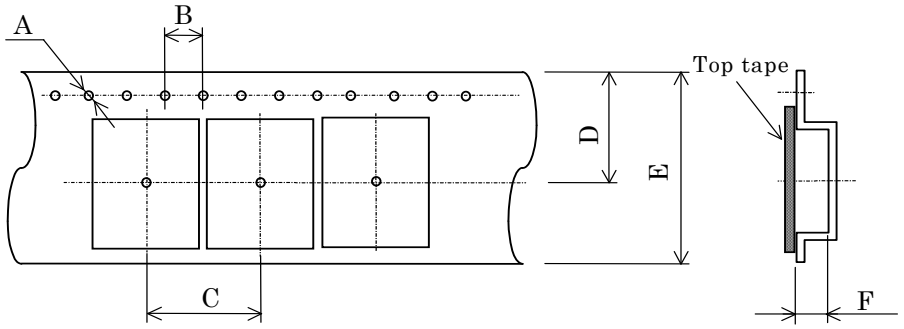
〔1〕 Taping specification

Subject to EIA-481& IEC 60286

(1) Tape dimensions TE-1612L

Material of the carrier tape : PS

Material of the top tape : PET

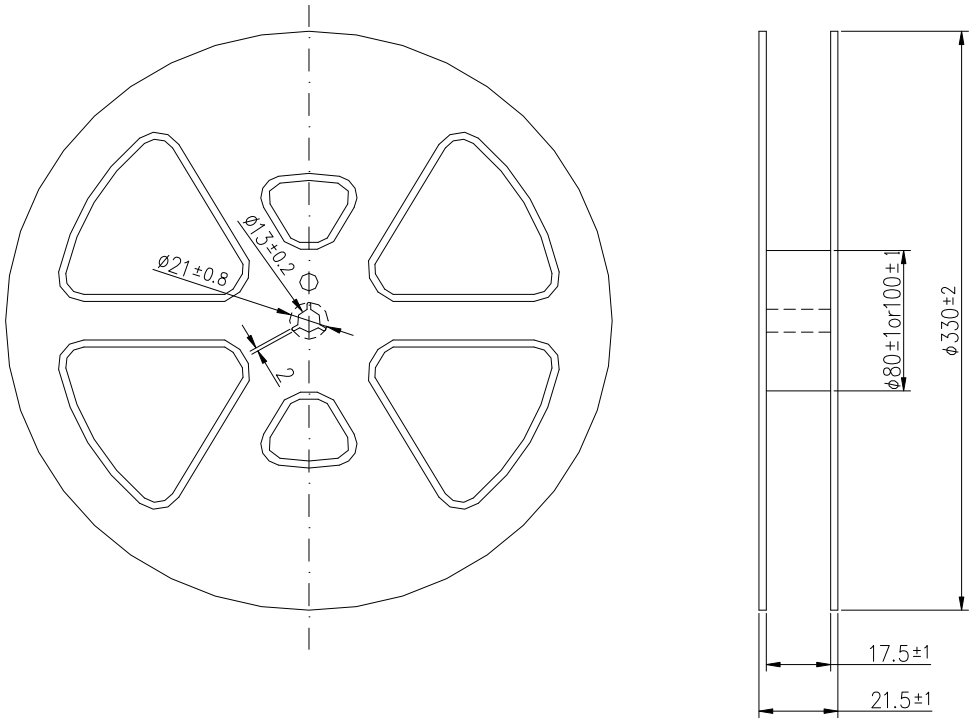


Symbol	A	B	C	D	E	F
Value	ϕ 1.5	4.0	12.0	9.25	16.0	3.65

Unit : mm

(2) Reel dimensions

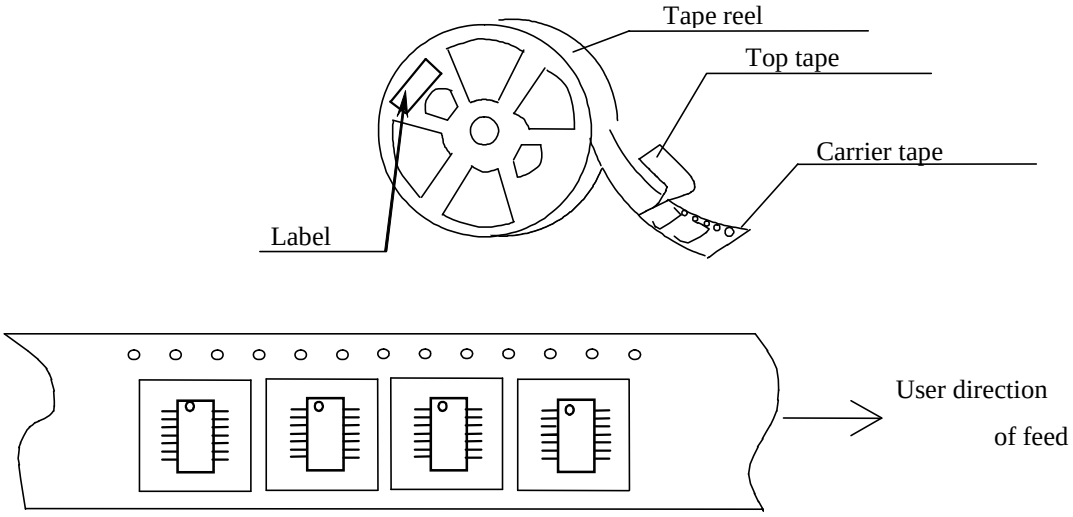
Material of the reel : Conductive polystyrene



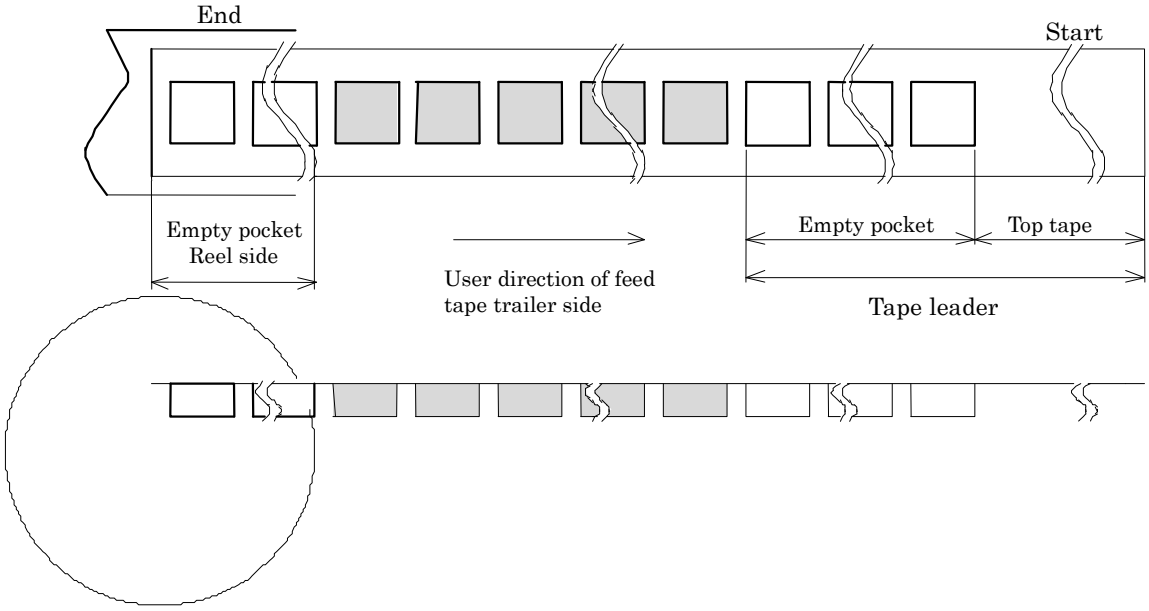
Form and Size of reel window shows are one of the example

(3) Packing

①Tape & reel



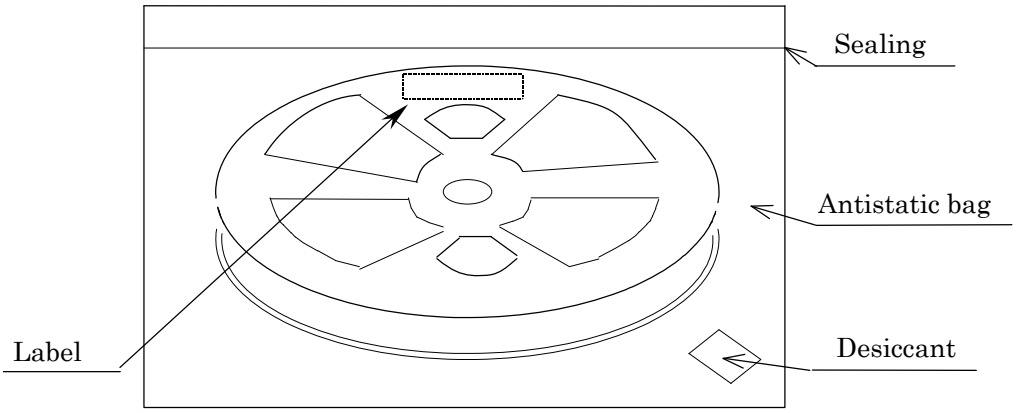
②Start & end point



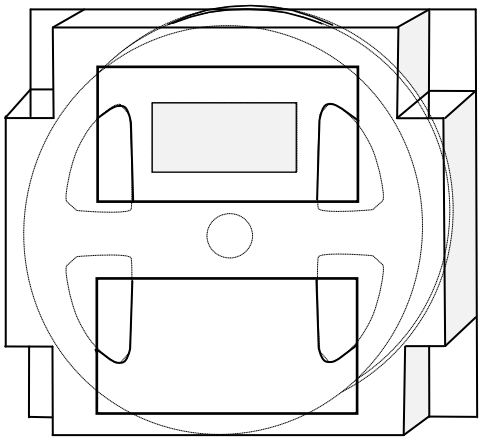
Item		Empty space
Tape leader	Top tape	Min. 1 000 mm
	Carrier tape	Min. 120 mm
Tape trailer	Top tape	Min. 0 mm
	Carrier tape	Min. 120 mm

〔2〕 Inner sleeve

a) Packing to antistatic bag

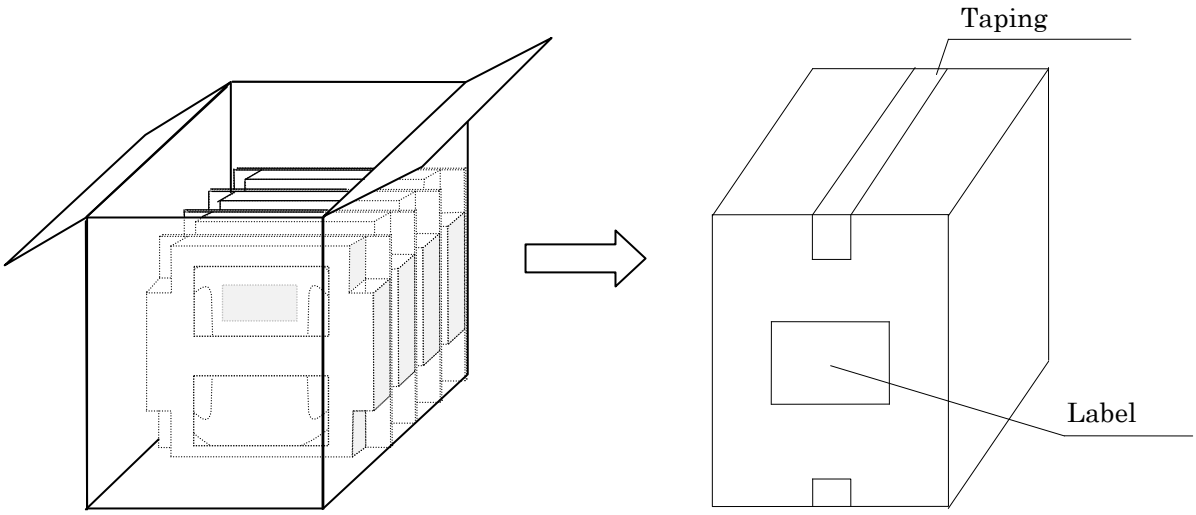


b) Packing to inner Sleeve



* There is also a case to put the two reel.

〔3〕 Shipping carton



〔4〕 Marking

(1) Reel marking

・Reel marking shall consist of :

1) Parts name
2) Quantity
3) Manufacturing date or symbol
4) Manufacturer’s date or symbol
5) Others (if necessary)

(2) Shipping carton marking

・Shipping carton marking shall consist of :

1) Parts name
2) Quantity

〔5〕 Quantity

・1 000 pcs./reel

〔6〕 Storage environment

(1) To storage the reel at 15 °C to 35 °C, 25 %RH to 85 %RH of humidity.
(2) To open the packing just before using.
(3) Not to expose the sun.
(4) Not to storage with some erosive chemicals.
(5) Nothing is allowed to put on the reel or carton to prevent mechanical damage.

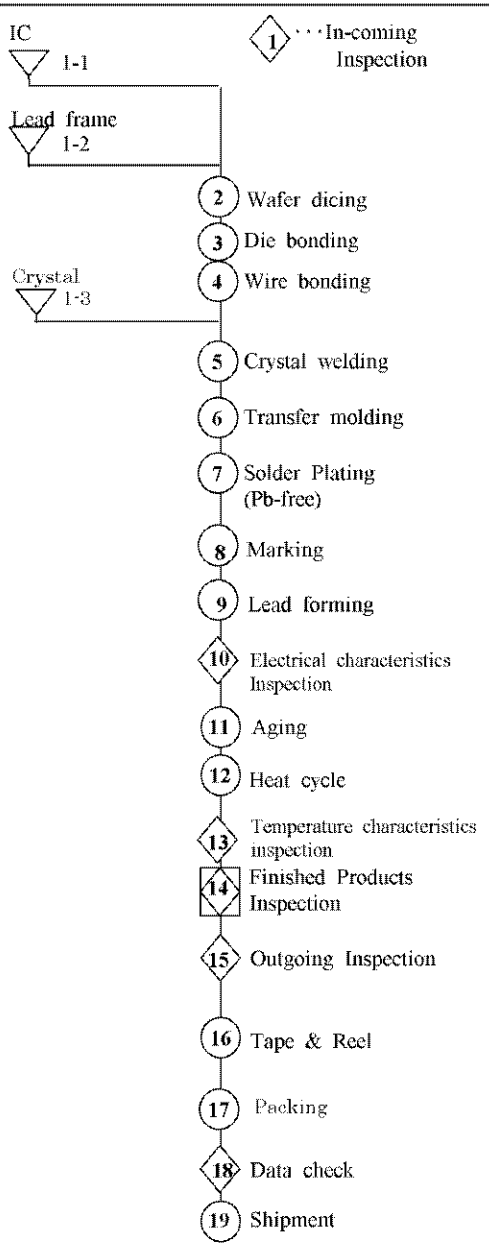
〔7〕 Handling

・To handle with care to prevent the damage of tape, reel and products.

- PROCESS QUALITY CONTROL -

No. SOP14-RB-PbF-ATE-1 **Real Time Clock Module SOP 14pin**

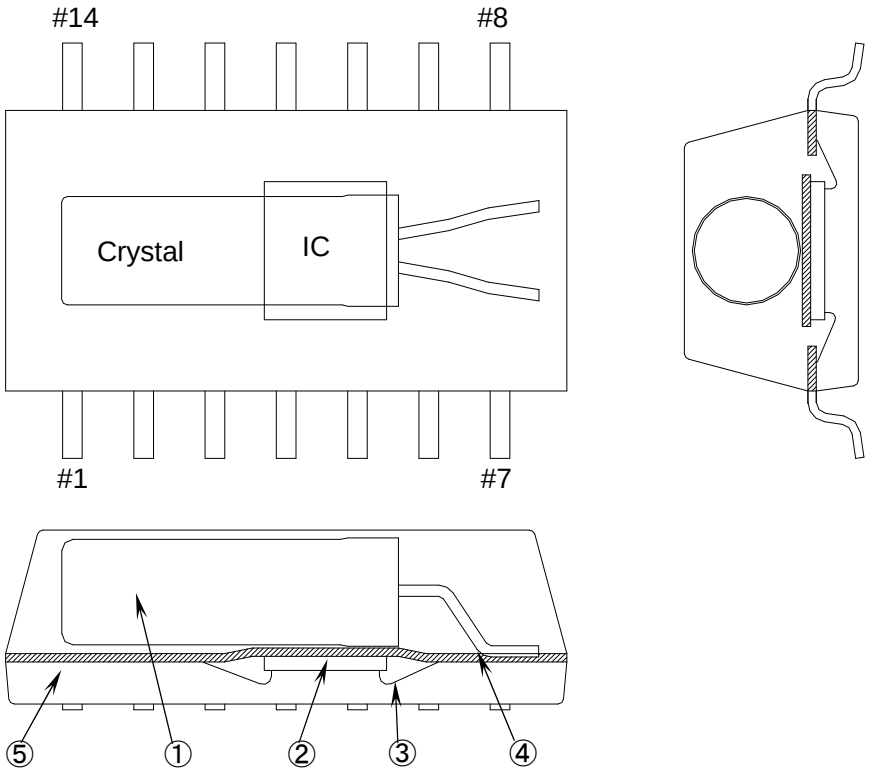
2015.05.14
RASA_Q_0001



No.	Section In charge	Standards & Specifications	Inspection & Control Item	Inspection Instruments	Inspection methods	Record
1	QA section	Purchasing specification Incoming Inspection standard	Appearance Dimension	Microscope	Sampling	Data Sheet
1-1	Subcontractor	Incoming Inspection standard	Model,Quantity	Visual inspection	Sampling	Data sheet
1-2	Subcontractor	Incoming Inspection standard	Model,Quantity, Appearance	Visual inspection	Sampling	Data sheet
2	Subcontractor	Assemble specification	Appearance	Visual inspection	Sampling	Data sheet
3	Subcontractor	Assemble specification	Appearance (chip/paste) Die shear strength Baking temperature,time	Microscope ,Visual inspection Pull-Gsuge Thermometer,Timer	Sampling	Data sheet
4	Subcontractor	Assemble specification	Wire-pull strength Bonding strength U.S.power Temperature,Force Appearance	Pull-tester Ball-share tester Thermometer,Gauge Dial-gauge Microscope	Sampling	Data sheet
1-3	Subcontractor	Incoming inspection standerd	Model,Quantity	Visual inspection	Sampling	Data sheet
5	Subcontractor	Assemble specification	Welding-power Pressure,Crystal position	Power-measure Gauge	Sampling	Data sheet
			Appearance	Microscope	100% Inspection	
6	Subcontractor	Assemble specification	Shape of bonded wire Mould Die-temperature Curing-Temperature,Time	Surface-thermometer Thermometer,Timer X-ray	Sampling	Data sheet
			Appearance	Visual Inspection	100% Inspection	
7	Subcontractor	Assemble specification	Belt speed, Time,Tact Plating thickness, Solder ability	Timer,Thermometer Fluorescent X-ray Microscope	Sampling	Data sheet
			Appearance	Visual inspection		
8	Subcontractor	Assemble specification	Appearance	Visual inspection	Sampling	Data sheet
9	Subcontractor	Assemble specification	Appearance Outer Dimention	Microscope	Sampling	Data sheet
10	Subcontractor	Manufacturing Instruction Sheet	Electrical characteristics	Measuring equipment	100% Inspection	Data sheet
11	Subcontractor	Manufacturing Instruction Sheet	Temperature,Time	Thermometer,Timer	Every lot	Data sheet
12	Subcontractor	Manufacturing Instruction Sheet	Temperature,Time	Thermometer,Timer	Every lot	Data sheet
13	Subcontractor	Manufacturing Instruction Sheet	Frequency Temperature characteristics	Measuring equipment	100% Inspection	Data sheet
14	Subcontractor	Manufacturing Instruction Sheet	Electrical characteristics	Measuring equipment	100% Inspection	Data sheet
15	Subcontractor	Inspection standard	Electrical characteristics Appearance	Measuring equipment Visual inspection	Sampling	Data sheet
16	Subcontractor	Assemble specification	Tape peel strength	Peel strength tester	Sampling	Data sheet
			Products direction	Camera detection	100% Inspection	
17	Subcontractor	Assemble specification	------	------	------	------
18	QA section	Specification sheet	Specification Appearance	------	Every lot	------
19	Production control section	Manufacturing Instruction sheet Daily shipping list	Customers Type Quantity	------	------	------

Structure Diagram 構造図

Model 型式	**SA package**	RTC / RX / RA / SG series
Document No. 管理№	-	SA_D_0001



⑤	Transfer molding compound モールド	
④	Lead Frame リードフレーム	
③	Bonding wire ボンディングワイヤ	
②	IC	
①	Crystal Unit 水晶振動子	
No.	Name of Part 部品名	

EPSON
EXCEED YOUR VISION

RELIABILITY TEST DATA

Product Name : RA-SA Series J-STD-020C

The Company evaluation condition

We evaluate environmental and mechanical characteristics by the following test condition . No. F-G-0622-04-005E

No.	ITEM	TEST CONDITIONS	VALUE *1		TEST Qty [n]	FAIL Qty [n]
			Δ f / f *2 [1 × 10^{-6}]	Electrical characteristics		
1	High temperature storage	+125 °C × 1 000 h	*3 ± 20	Satisfy specification after test	22	0
2	Low temperature storage	-55 °C × 1 000 h	*3 ± 20		22	0
3	High temperature bias	+125 °C × 5.5 V × 1 000 h	*3 ± 20		22	0
4	Low temperature bias	-40 °C × 5.5 V × 1 000 h	*3 ± 20		22	0
5	Temperature humidity bias	+85 °C × 85 %RH × 5.5 V × 1 000 h	*3 ± 20		22	0
6	Temperature cycle	-40 °C ⇔ +125 °C 30 min at each temp. 1 000 cycles	*3 ± 20		22	0
7	Resistance to soldering heat	**Reflow furnace with the condition 3times JEDECJ-STD-020C**	± 8		22	0
8	Drop	Free drop from 750 mm height on a hard wooden board for 3 times (Board is thickness more than 30 mm)	± 5		22	0
9	Vibration	10 Hz to 55 Hz amplitude 0.75 mm 55 Hz to 500 Hz acceleration 98 m/s2 10 Hz → 500 Hz → 10 Hz 15 min/cycle 6 h (2 h × 3 directions)	± 5		22	0
10	Solderability	Dip termination into solder bath at +235 °C ± 5 °C for 5 s (Using Rosin Flux)	Termination must be 95 % covered with fresh solder		11	0

Notes

*1 Each test done independently.

*2 Measuring 2 h to 24 h later leaving in room temperature after each test.

*3 Pre-conditions (Dry +125℃x24h→ high temp & humidity +85℃x85%RHx168h→Reflow 3times) should be performed before each tests. Pre conditionings Initial value shall be after 24 h at room temperature.

Qualification Data

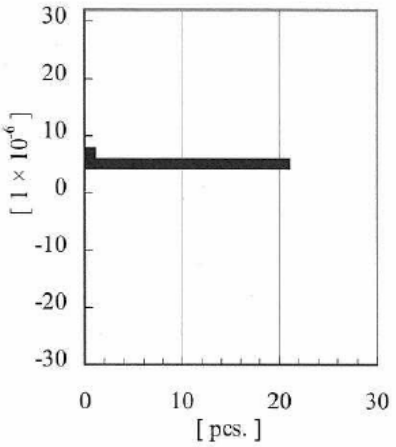
EPSON
EXCEED YOUR VISION

Product Name : RA-SA Series J-STD-020C

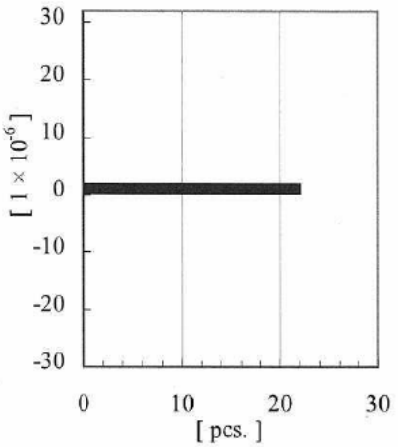
Frequency Shift Rate Δ f / f

No. F-G-0622-04-006E

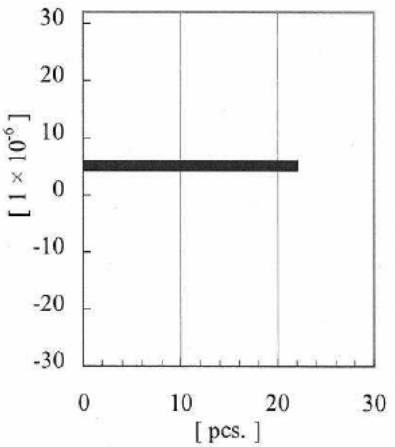
1. High temp. storage
+125 °C × 1 000 h



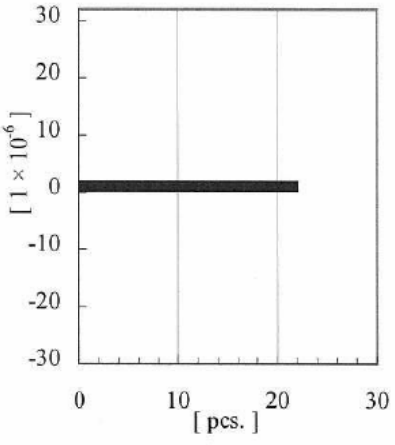
2. Low temp. storage
-55 °C × 1 000 h



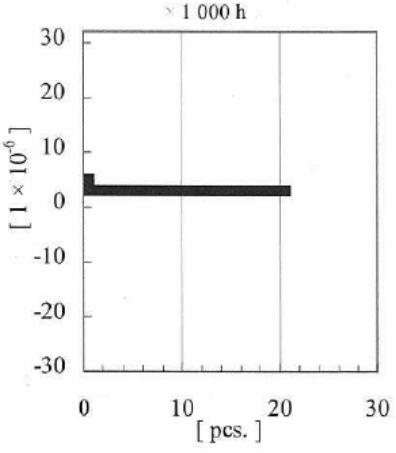
3. High temp. bias
+125 °C × 5.5 V × 1 000 h



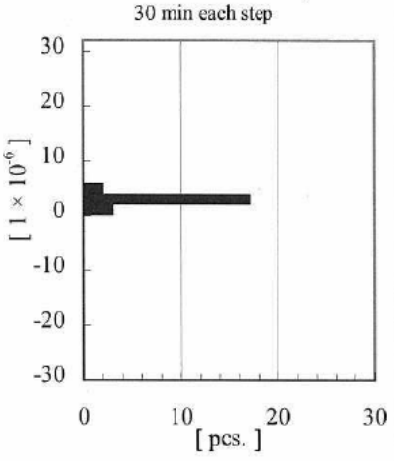
4. Low temp. bias
-40 °C × 5.5 V × 1 000 h



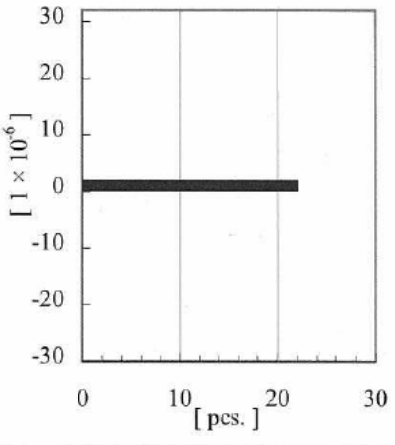
5. Temp. humidity bias
+85 °C × 85 %RH × 5.5 V
× 1 000 h



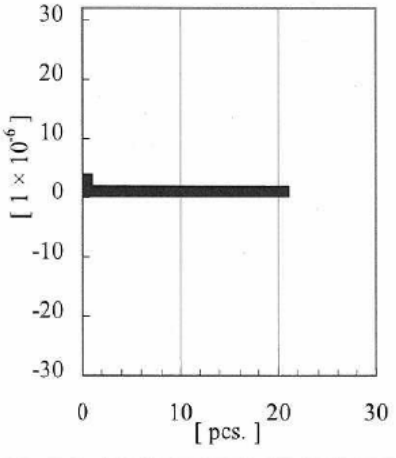
6. Temp. cycle
-40 °C ⇔ +125 °C × 1 000 cycles
30 min each step



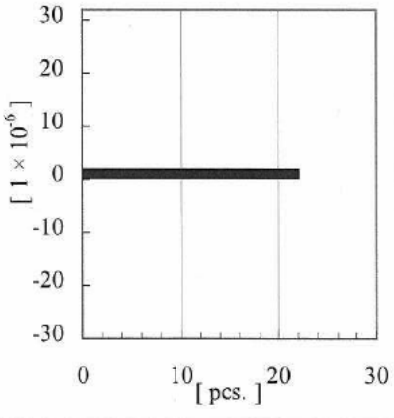
7.Resistance to soldering heat
For convention reflow
soldering furnace (3 times)



8. Drop
750 mm x 3Times



9. Vibration
10 Hz to 55 Hz amplitude 0.75 mm
55 Hz to 500 Hz 98 m/s²
15 min / cycle 6 h (2 h × 3 directions)



Qualification Data