

SH PATEO ELE EQUIPMENT MANU

RECIPIENT

SPECIFICATIONS

Product No. : X1B000262000200

MODEL : RA8803SA

SPEC. No. : Q13-171-1B

DATE: Dec. 24. 2013

SEIKO EPSON CORPORATION

8548 Naka-minowa
Minowa-machi Kamiina-gun
Nagano-ken
399-4696 Japan

CHECKED H. Koike / TD Production Engineering Department Manager
Hideki Koike

CHECKED T. Tonouchi / TD Production Engineering Department Senior Staff
Tetsuji Tonouchi

CHECKED Y. Hiraizumi / TD-CS Quality Assurance Department Manager
Yasushi Hiraizumi

PREPARED T. Kurumizawa / TD-CS Quality Assurance Department Senior Staff
Takashi kurumizawa

SPECIFICATION

1. Application

- 1) This document is applicable to the real time clock module RA8803SA that are delivered to SH PATEO ELE EQUIPMENT MANU from Seiko Epson Corp.
- 2) RoHS compliant
RA8803SA contains lead in high melting type solder which is exempted in RoHS directive.
- 3) This Product supplied (and any technical information furnished, if any) by Seiko Epson Corporation shall not be used for the development and manufacture of weapon of mass destruction or for other military purposes. Making available such products and technology to any third party who may use such products or technologies for the said purposes are also prohibited.
- 4) This product listed here is designed as components or parts for electronics equipment in general consumer use. We do not expect that any of these products would be incorporated or otherwise used as a component or part for the equipment, which requires an systems, and medical equipment, the functional purpose of which is to keep extra high reliability, such as satellite, rocket and other space life.

This RA8803SA is authorized for Navigation system for automobile only.

2. Product No. / Model

The product No. of this real time clock module is X1B000262000200.
The model is RA8803SA.

3. Packing

It is subject to the packing standard of Seiko Epson Corp.

4. Warranty

Defective parts which are originated by us are replaced free of charge in case defects are found within 12 Months after delivery.

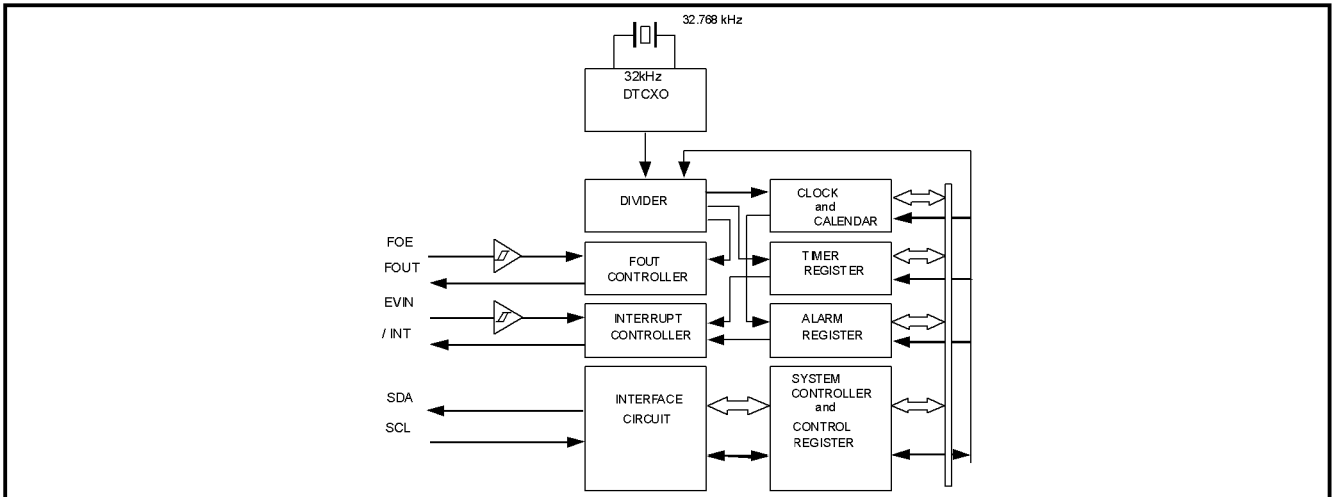
5. Amendment and abolishment

Amendment and/or abolishment of this specification are subject to the agreement of both parties.

6. Contents

Item No.	Item	Page
1	Block diagram	2
2	Register table	2 to 3
3	Terminal description	4
4	External Dimensions / Marking Layout	5
5	Absolute maximum ratings	6
6	Recommended Operating Conditions	6
7	Frequency characteristics	6
8	Electrical characteristics	7 to 8
9	Environmental and mechanical characteristics	9
10	Reading/Writing Data via the I ² C Bus Interface	10 to 11
11	Note	12

1. Block Diagram



2. Description of Registers

2.1. Write / Read and Bank Select

Address 00h to 0Fh : Basic time and calendar register ... Compatible with RX-8801.

Address 10h to 1Fh : Extension register1 ... Adds 1/100s Counter.

Address 20h to 2Fh : Extension register2 ... Capture buffer and Event control registers.

2.2. Register table (Basic time and calendar register)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
00	SEC	○	40	20	10	8	4	2	1	P	P
01	MIN	○	40	20	10	8	4	2	1	P	P
02	HOUR	○	○	20	10	8	4	2	1	P	P
03	WEEK	○	6	5	4	3	2	1	0	P	P
04	DAY	○	○	20	10	8	4	2	1	P	P
05	MONTH	○	○	○	10	8	4	2	1	P	P
06	YEAR	80	40	20	10	8	4	2	1	P	P
07	RAM	•	•	•	•	•	•	•	•	P	P
08	MIN Alarm	AE	40	20	10	8	4	2	1	P	P
09	HOUR Alarm	AE	•	20	10	8	4	2	1	P	P
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	P	P
	DAY Alarm		•	20	10	8	4	2	1		
0B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
0C	Timer Counter 1	•	•	•	•	2048	1024	512	256	P	P
0D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
0E	Flag Register	○	○	UF	TF	AF	EVF	VLF	VDET	P	P
0F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	EIE	○	RESET	P	P

P : Possible , I : Impossible

Note When after the initial power-up or when the result of read out the VLF bit is "1", initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

- *1) During the initial power-up, the TEST bit is reset to "0" and the VLF bit is set to "1".
* At this point, all other register values are undefined, so be sure to perform a reset before using the module.
- *2) Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.
- *3) Any bit marked with "○" should be used with a value of "0" after initialization.
- *4) Any bit marked with "•" is a RAM bit that can be used to read or write any data.
- *5) The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

2.3. Register table (Extension register1)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
10	1/100 S	80	40	20	10	8	4	2	1	P	I
11	SEC	○	40	20	10	8	4	2	1	P	P
12	MIN	○	40	20	10	8	4	2	1	P	P
13	HOUR	○	○	20	10	8	4	2	1	P	P
14	WEEK	○	6	5	4	3	2	1	0	P	P
15	DAY	○	○	20	10	8	4	2	1	P	P
16	MONTH	○	○	○	10	8	4	2	1	P	P
17	YEAR	80	40	20	10	8	4	2	1	P	P
18	MIN Alarm	AE	40	20	10	8	4	2	1	P	P
19	HOUR Alarm	AE	●	20	10	8	4	2	1	P	P
1A	WEEK Alarm	AE	6	5	4	3	2	1	0	P	P
	DAY Alarm		●	20	10	8	4	2	1		
1B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	P	P
1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
1E	Flag Register	○	○	UF	TF	AF	EVF	VLF	VDET	P	P
1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	EIE	○	RESET	P	P

1/100S Reg. is cleared to "00" by writing in the SEC Reg. or RESET bit and the ERST bit operation.

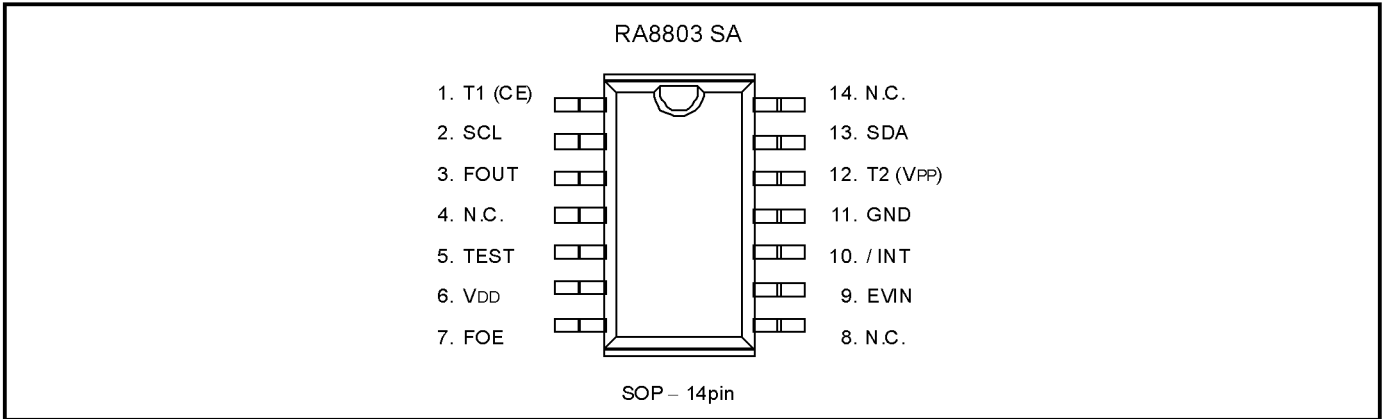
2.4. Register table (Extension register2)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
20	1/100 S CP	80	40	20	10	8	4	2	1	P	I
21	SEC CP	○	40	20	10	8	4	2	1	P	I
22	-	-	-	-	-	-	-	-	-	-	-
23	-	-	-	-	-	-	-	-	-	-	-
24	-	-	-	-	-	-	-	-	-	-	-
25	-	-	-	-	-	-	-	-	-	-	-
26	-	-	-	-	-	-	-	-	-	-	-
27	-	-	-	-	-	-	-	-	-	-	-
28	-	-	-	-	-	-	-	-	-	-	-
29	-	-	-	-	-	-	-	-	-	-	-
2A	-	-	-	-	-	-	-	-	-	-	-
2B	-	-	-	-	-	-	-	-	-	-	-
2C	OSC Offset	○	○	○	○	OFS3	OFS2	OFS1	OFS0	P	P
2D	-	-	-	-	-	-	-	-	-	-	-
2E	-	-	-	-	-	-	-	-	-	-	-
2F	Event Control	ECP	EHL	ET1	ET0	○	○	○	ERST	P	P

When an initial power on, frequency offset is ± 0 selected by "0000".

3. Terminal description

3.1. Terminal connections



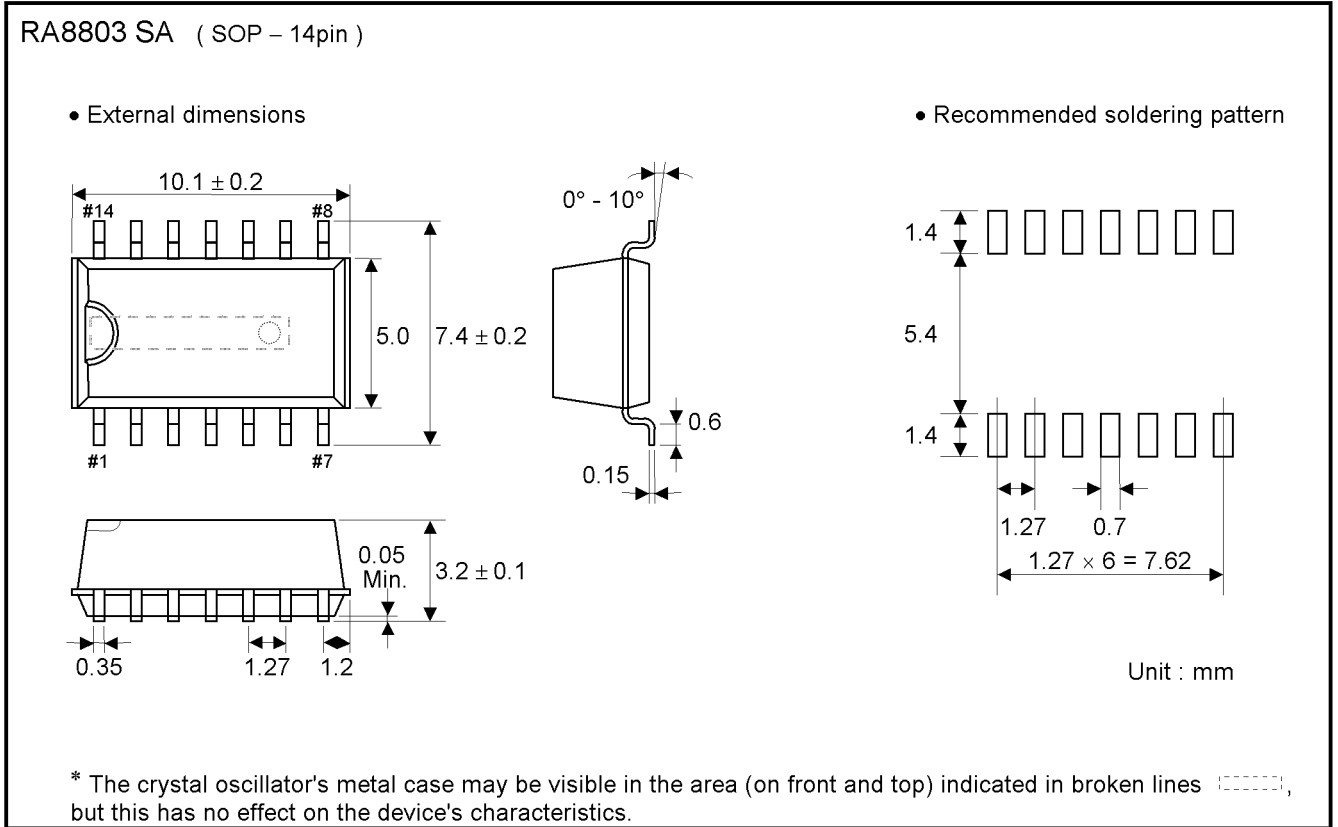
3.2. Pin Functions

Signal name	I/O	Function
SDA	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I ² C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.
SCL	Input	This is the serial clock input pin for I ² C Bus communications.
FOUT	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. When output is stopped, the FOUT pin = "Hi-Z"(high impedance).
FOE	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
/INT	Output	This pins is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
EVIN	Input	External event input pin.
VDD	–	This pin is connected to a positive power supply.
GND	–	This pin is connected to a ground.
TEST	Input	Use by the manufacture for testing. (Do not connect externally.)
T1 (CE)	Input	Use by the manufacture for testing. (Do not connect externally.)
T2 (VPP)	–	Use by the manufacture for testing. (Do not connect externally.)
N.C.	–	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.

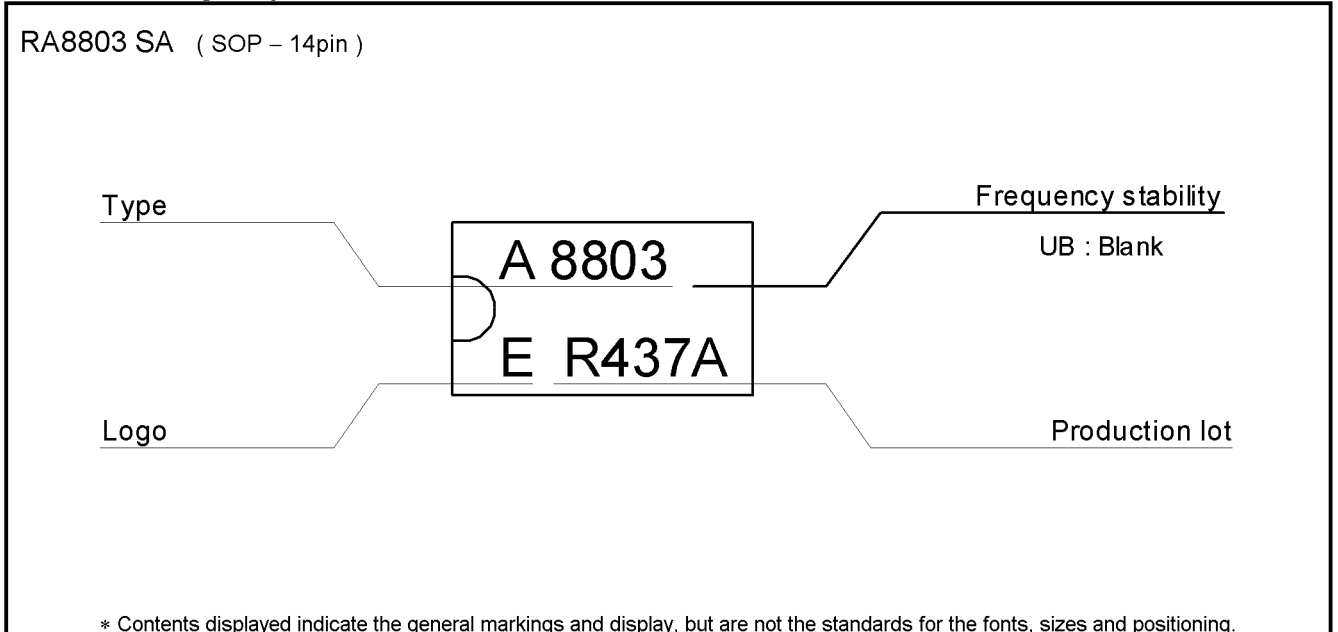
Note: Be sure to connect a bypass capacitor rated at least 0.1 μF between VDD and GND.

4. External Dimensions / Marking Layout

4.1 External Dimensions



4.2 Marking Layout



5. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	VDD	Between VDD and GND	-0.3 to +6.5	V
Input voltage (1)	VIN1	FOE pin	GND-0.3 to VDD+0.3	V
Input voltage (2)	VIN2	SCL and SDA pins	GND-0.3 to +6.5	V
Output voltage (1)	VOUT1	FOUT pin	GND-0.3 to VDD+0.3	V
Output voltage (2)	VOUT2	SDA and /INT pins	GND-0.3 to +6.5	V
Storage temperature	TSTG	When stored separately, without packaging	-55 to +125	°C

6. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VDD	Interface voltage	1.6	3.0	5.5	V
Temp. compensation voltage	VTEM	Temperature compensation voltage	2.2	3.0	5.5	V
Clock supply voltage	VCLK	-	1.6	3.0	5.5	V
Operating temperature	TOPR	No condensation	-40	+25	+85	°C

7. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition		Rating	Unit
Frequency stability	$\Delta f / f$	U B	Ta= 0 to +50 °C, VDD=3.0 V Ta=-40 to +85 °C, VDD=3.0 V	± 3.8 (*1) ± 5.0 (*2)	$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta= +25 °C, VDD=2.2 V to 5.5 V		± 1.0 Max.	$\times 10^{-6} / V$
Oscillation start time	tSTA	Ta= +25 °C, VDD=1.6 V Ta=-40 to +85 °C, VDD=1.6 V to 5.5 V		1.0 Max. 3.0 Max.	s
Aging	fa	Ta= +25 °C, VDD=3.0 V, first year		± 3 Max.	$\times 10^{-6}$ / year

*1) Equivalent to 10 seconds of month deviation. *2) Equivalent to 13 seconds of month deviation. (excluding offset)

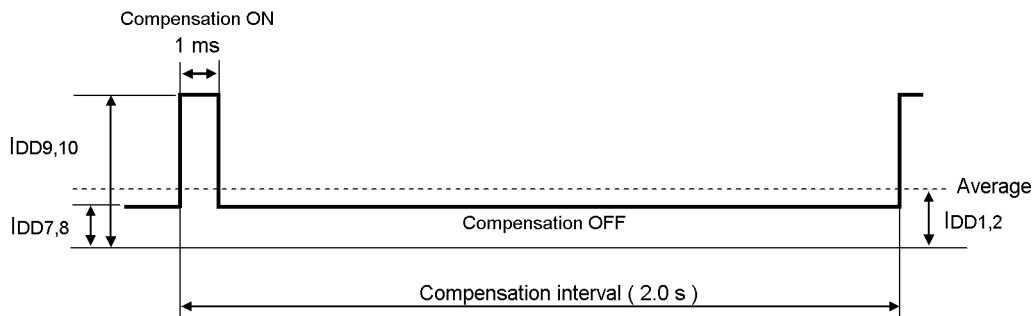
8. Electrical Characteristics

8.1. DC Characteristics

*Unless otherwise specified, GND = 0 V, VDD = 1.6 V to 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	IDD1	f _{scl} = 0 Hz, / INT = VDD FOE = GND FOUT : output OFF (High Z) Compensation interval 2.0 s	VDD = 5 V		0.75	3.4	μA
Current consumption (2)	IDD2		VDD = 3 V		0.75	2.1	
Current consumption (3)	IDD3	f _{scl} = 0 Hz, / INT = VDD FOE = VDD FOUT :32.768 kHz, CL =0pF Compensation interval 2.0 s	VDD = 5 V		2.0	7.5	μA
Current consumption (4)	IDD4		VDD = 3 V		1.5	5.0	
Current consumption (5)	IDD5	f _{scl} = 0 Hz, / INT = VDD FOE = VDD FOUT :32.768 kHz, CL =30pF Compensation interval 2.0 s	VDD = 5 V		7.0	20.0	μA
Current consumption (6)	IDD6		VDD = 3 V		4.5	12.0	
Current consumption (7)	IDD7	f _{scl} = 0 Hz, / INT = VDD FOE = GND FOUT : output OFF (High Z) Compensation OFF	VDD = 5 V		0.7	2.95	μA
Current consumption (8)	IDD8		VDD = 3 V		0.7	1.85	
Current consumption (9)	IDD9	f _{scl} = 0 Hz, / INT = VDD FOE = GND FOUT : output OFF (High Z) Compensation ON (peak)	VDD = 5 V		120	900	μA
Current consumption (10)	IDD10		VDD = 3 V		115	350	
High-level input voltage	VIH	CE, DI, CLK, FOE, EVIN pins		0.8 × VDD		6.5	V
Low-level input voltage	VIL	CE, DI, CLK, FOE, EVIN pins		GND - 0.3		0.2 × VDD	V
High-level output voltage	VOH1	FOUT pin	VDD=5 V, IOH=-1 mA	4.5		5.0	V
	VOH2		VDD=3 V, IOH=-1 mA	2.2		3.0	
	VOH3		VDD=3 V, IOH=-100 μA	2.9		3.0	
Low-level output voltage	VOL1	FOUT pin	VDD=5 V, IOL=1 mA	GND		GND+0.5	V
	VOL2		VDD=3 V, IOL=1 mA	GND		GND+0.8	
	VOL3		VDD=3 V, IOL=100 μA	GND		GND+0.1	
	VOL4	/ INT pin	VDD=5 V, IOL=1 mA	GND		GND+0.25	V
	VOL5	/ INT pin	VDD=3 V, IOL=1 mA	GND		GND+0.4	V
	VOL6	SDA pin	VDD ≥ 2 V, IOL=3 mA	GND		GND+0.4	V
Input leakage current	ILK	FOE, SCL, SDA pins, VIN = VDD or GND		-0.5		0.5	μA
Output leakage current	IOZ	/ INT, SDA, FOUT pins, VOUT = VDD or GND		-0.5		0.5	μA

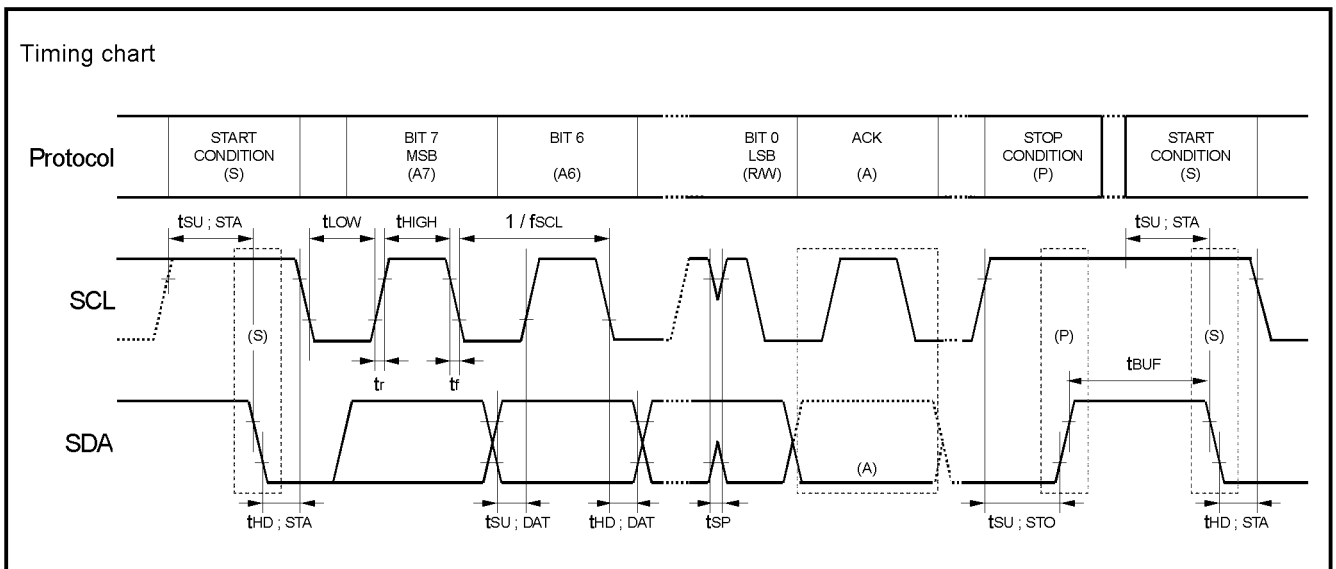
- Temperature compensation and consumption current



8.2. AC Characteristics

* Unless otherwise specified,
GND = 0 V, VDD = 1.8 V to 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL				400	kHz
Start condition setup time	tSU;STA		0.6			μs
Start condition hold time	tHD;STA		0.6			μs
Data setup time	tSU;DAT		100			ns
Data hold time	tHD;DAT		0		900	ns
Stop condition setup time	tSU;STO		0.6			μs
Bus idle time between start condition and stop condition	tBUF		1.3			μs
Time when SCL = "L"	tLOW		1.3			μs
Time when SCL = "H"	tHIGH		0.6			μs
Rise time for SCL and SDA	tr				0.3	μs
Fall time for SCL and SDA	tf				0.3	μs
Allowable spike time on bus	tSP				50	ns
FOUT duty	tW / t	50% of VDD level	40	50	60	%



Caution: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 0.95 seconds**. If such communication requires **0.95 seconds** or longer, the I²C bus interface is reset by the internal bus timeout function.

9. Environmental and mechanical characteristics

(The company evaluation condition We evaluate it by the following examination item and examination condition.)

No.	Item	Value *1		Test Conditions
		$\Delta f / f$ [1×10^{-6}] *2	Electrical characteristics	
1	High temperature storage	*3 \pm 50	*4 Satisfy item 7,8 after test	+125 °C \times 1 000 h
2	Low temperature storage	*3 \pm 10		-55 °C \times 1 000 h
3	High temperature bias	*3 \pm 20		+85 °C \times 5.5 V \times 1 000 h
4	Low temperature bias	*3 \pm 10		-40 °C \times 5.5 V \times 1 000 h
5	Temperature humidity bias	*3 \pm 20		+85 °C \times 85 %RH \times 5.5 V \times 1 000 h
6	Temperature cycle	*3 \pm 10		-40 °C \Leftrightarrow +85 °C 30 min at each temp. 1000 cycles
7	Resistance to soldering heat	\pm 8		IPC/JEDEC J-STD-020D.1 Reflow (3 times)
8	Drop	\pm 5		Free drop from 750 mm height on a hard wooden board for 3 times (Board is thickness more than 30 mm)
9	Vibration	\pm 5		10 Hz to 55 Hz amplitude 0.75 mm 55 Hz to 500 Hz acceleration 98 m/s ² 10 Hz \rightarrow 500 Hz \rightarrow 10 Hz 15min./cycle 6 h (2 hours , 3 directions)
10	Solderability	Termination must be 95 % covered with fresh solder		Dip termination into solder bath at +235 °C \pm 5 °C for 5 s (Using Rosin Flux)

< Notes >

*1 Each test done independently.

*2 Measuring 2 h to 24 h later leaving in room temperature after each test.

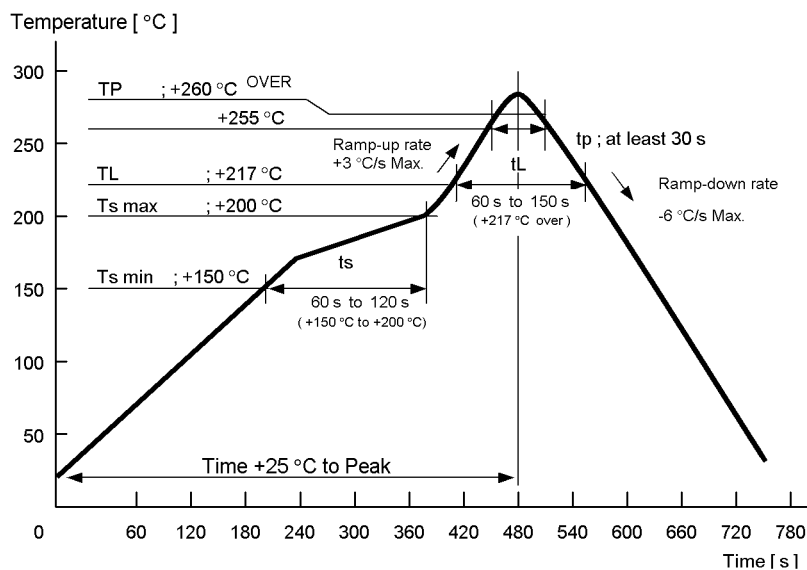
*3 Pre conditionings

- +125 °C \times 24 h to +85 °C \times 85 % \times 168 h \pm 1 h \rightarrow reflow 3 times
- Initial value shall be after 24 h at room temperature.

*4 7. Frequency Characteristics (but excludes frequency tolerance and aging.)

8. Electrical characteristics

◆ Reflow condition (follow to IPC / JEDEC J-STD-020D.1)



10. Reading/Writing Data via the I²C Bus Interface

10.1 Overview of I²C-BUS

10.1.1

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

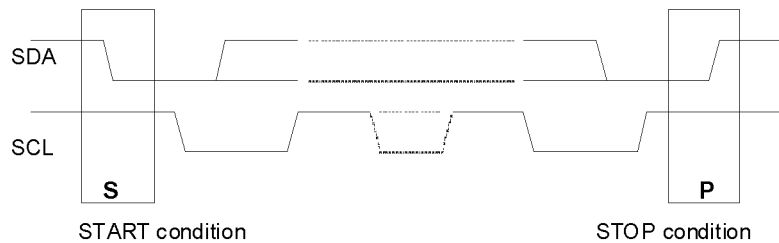
10.1.2

Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

10.1.3

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.



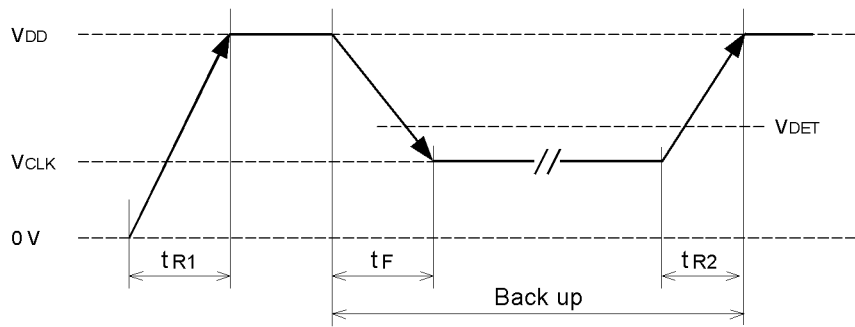
10.1.4. Slave address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device. All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is **[0110 010*]**. An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

	Transfer data	Slave address							R/W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	65 h	0	1	1	0	0	1	0	1 (= Read)
Write	64 h								0 (= Write)

10.2 Backup and Recovery



Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Power supply detection voltage (1)	V_{DET}	-			2.2	V
Power supply detection voltage (2)	V_{LOW}	-			1.6	V
Power supply drop time	t_F	-	2			$\mu s / V$
Initial power-up time	t_{R1}	-			10	ms / V
Clock maintenance power-up time	t_{R2}	$1.6V \rightarrow VDD \leq 3.6V$	5			$\mu s / V$
		$1.6V \rightarrow VDD > 3.6V$	15			$\mu s / V$

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater than 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 $^{\circ}\text{C}$, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

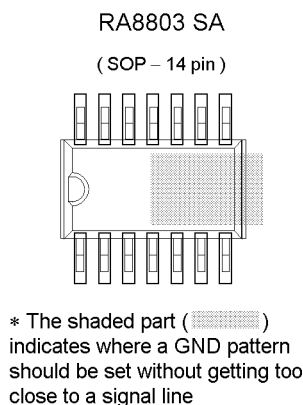
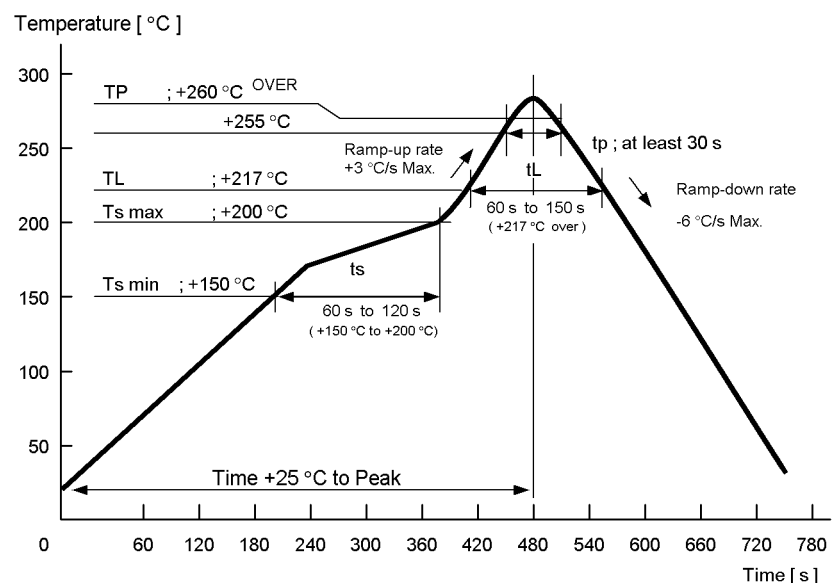


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



TAPING SPECIFICATION

I . Application

This standard will apply to SOP 14 pin package.

Spec : SA package

II . Contents

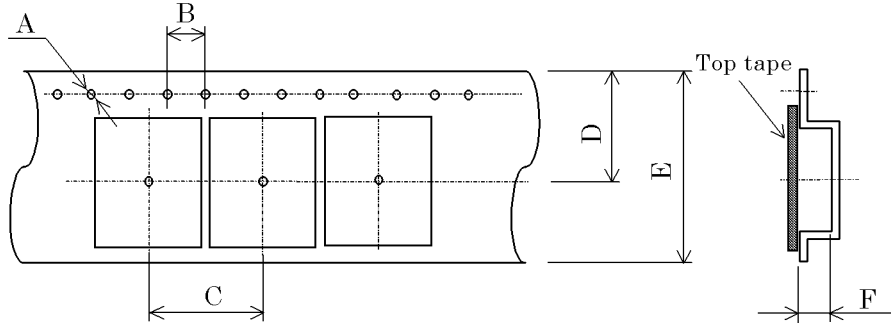
Item No.	Item	Page
[1]	Taping specification	1 to 2
[2]	Inner carton	3
[3]	Shipping carton	
[4]	Marking	4
[5]	Quantity	
[6]	Storage environment	
[7]	Handling	

[1] Taping specification

Subject to EIA-481& IEC 60286

(1) Tape dimensions TE-1612L

Material of the carrier tape : PS
 Material of the top tape : PET

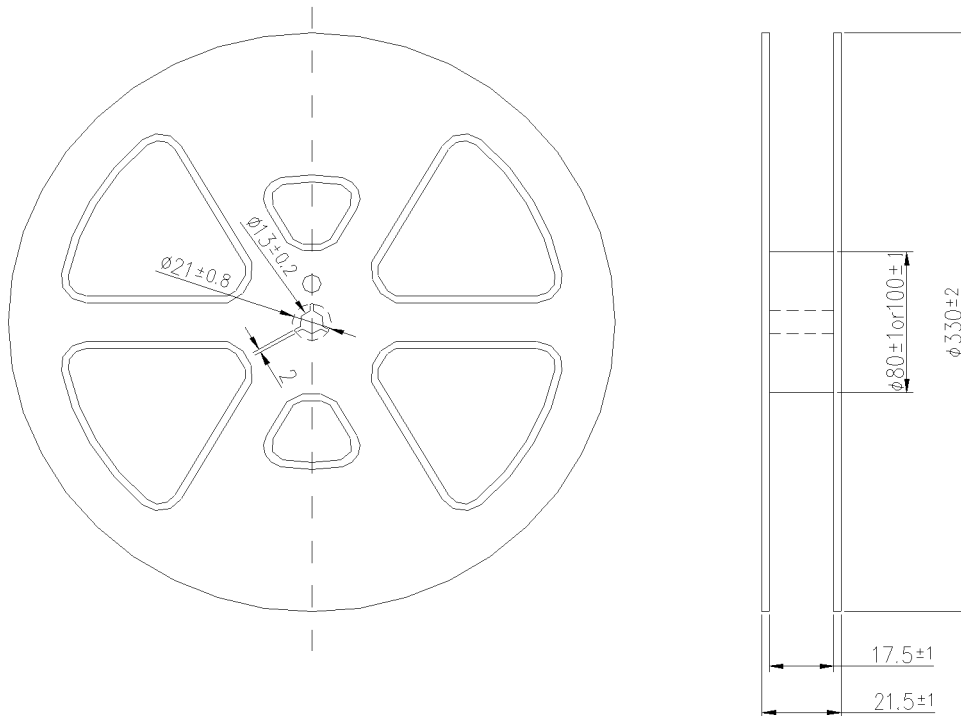


Symbol	A	B	C	D	E	F
Value	$\phi 1.5$	4.0	12.0	9.25	16.0	3.65

Unit : mm

(2) Reel dimensions

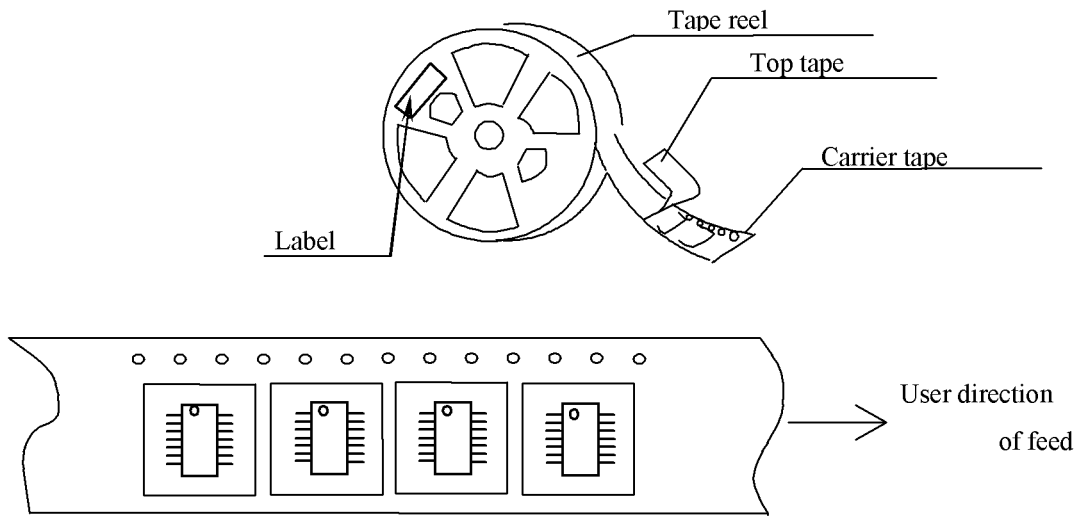
Material of the reel : Conductive polystyrene



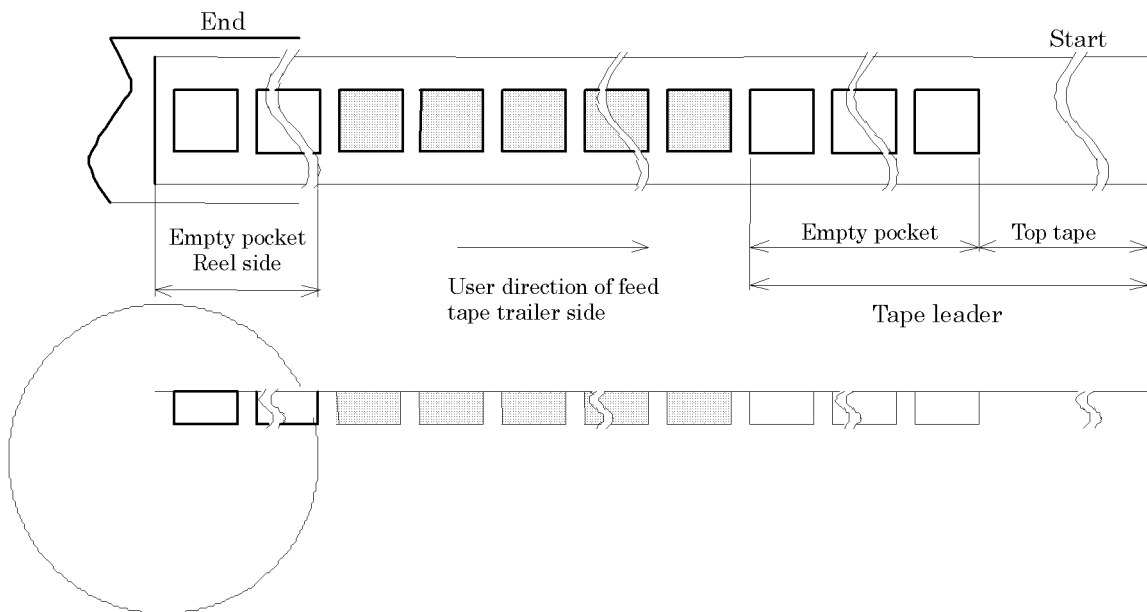
Form and Size of reel window shows are one of the example

(3) Packing

①Tape & reel



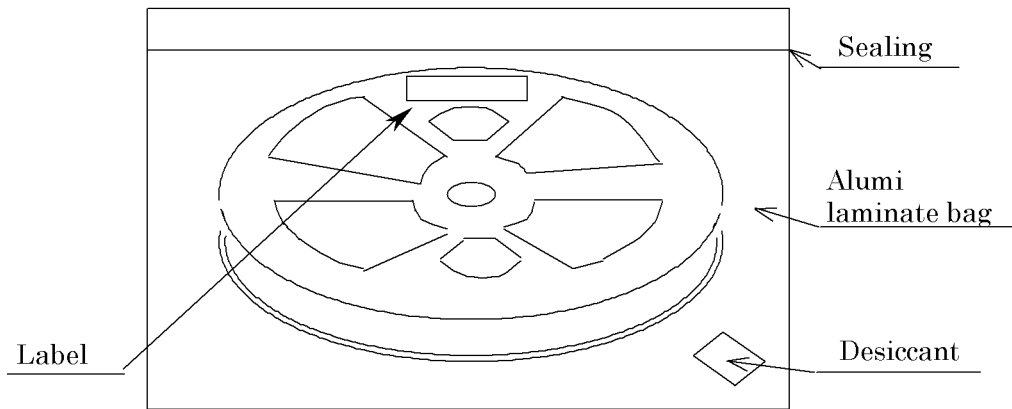
②Start & end point



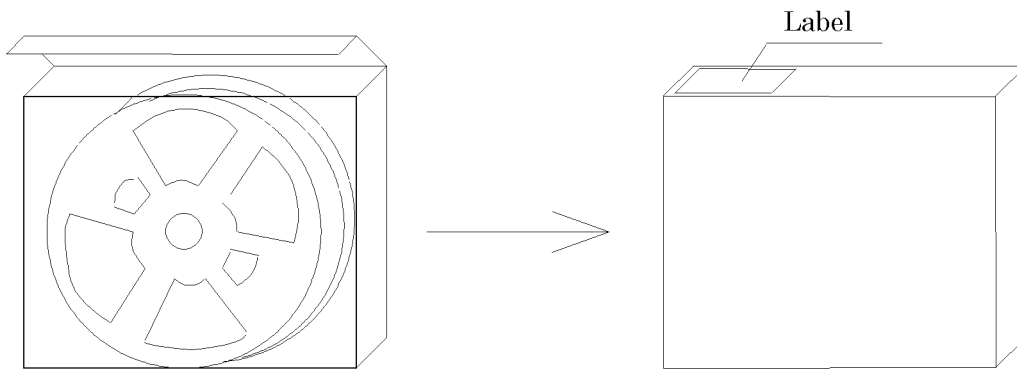
Item		Empty space
Tape leader	Top tape	Min. 1 000 mm
	Carrier tape	Min. 120 mm
Tape trailer	Top tape	Min. 0 mm
	Carrier tape	Min. 120 mm

[2] Inner carton

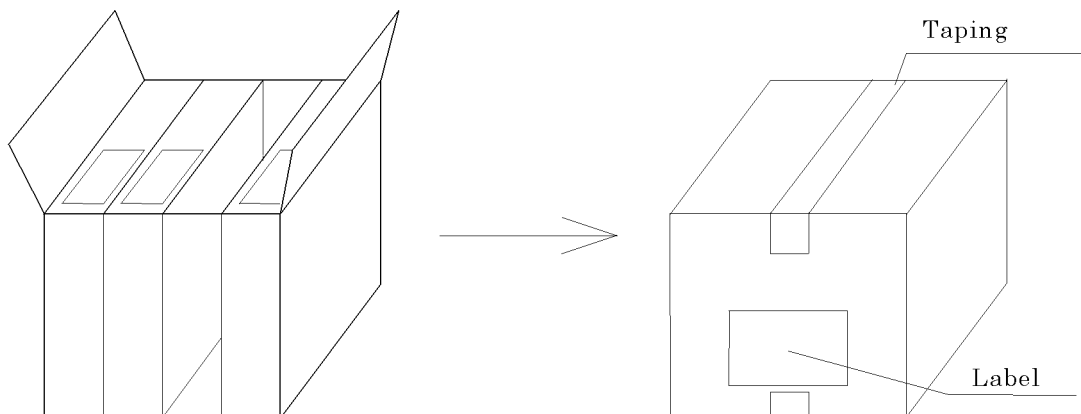
a) Packing to antistatic bag



b) Packing to inner carton



[3] Shipping carton



[4] Marking

(1) Reel marking

- Reel marking shall consist of :

- 1) Parts name
- 2) Quantity
- 3) Manufacturing date or symbol
- 4) Manufacturer's date or symbol
- 5) Others (if necessary)

(2) Inner carton marking

- Same as reel marking.

(3) Shipping carton marking

- Shipping carton marking shall consist of :

- 1) Parts name
- 2) Quantity

[5] Quantity

- 1 000 pcs./reel

[6] Storage environment

- (1) To storage the reel at 15 °C to 35 °C, 25 %RH to 85 %RH of humidity.
- (2) To open the packing just before using.
- (3) Not to expose the sun.
- (4) Not to storage with some erosive chemicals.
- (5) Nothing is allowed to put on the reel or carton to prevent mechanical damage.

[7] Handling

- To handle with care to prevent the damage of tape, reel and products.

- PROCESS QUALITY CONTROL -

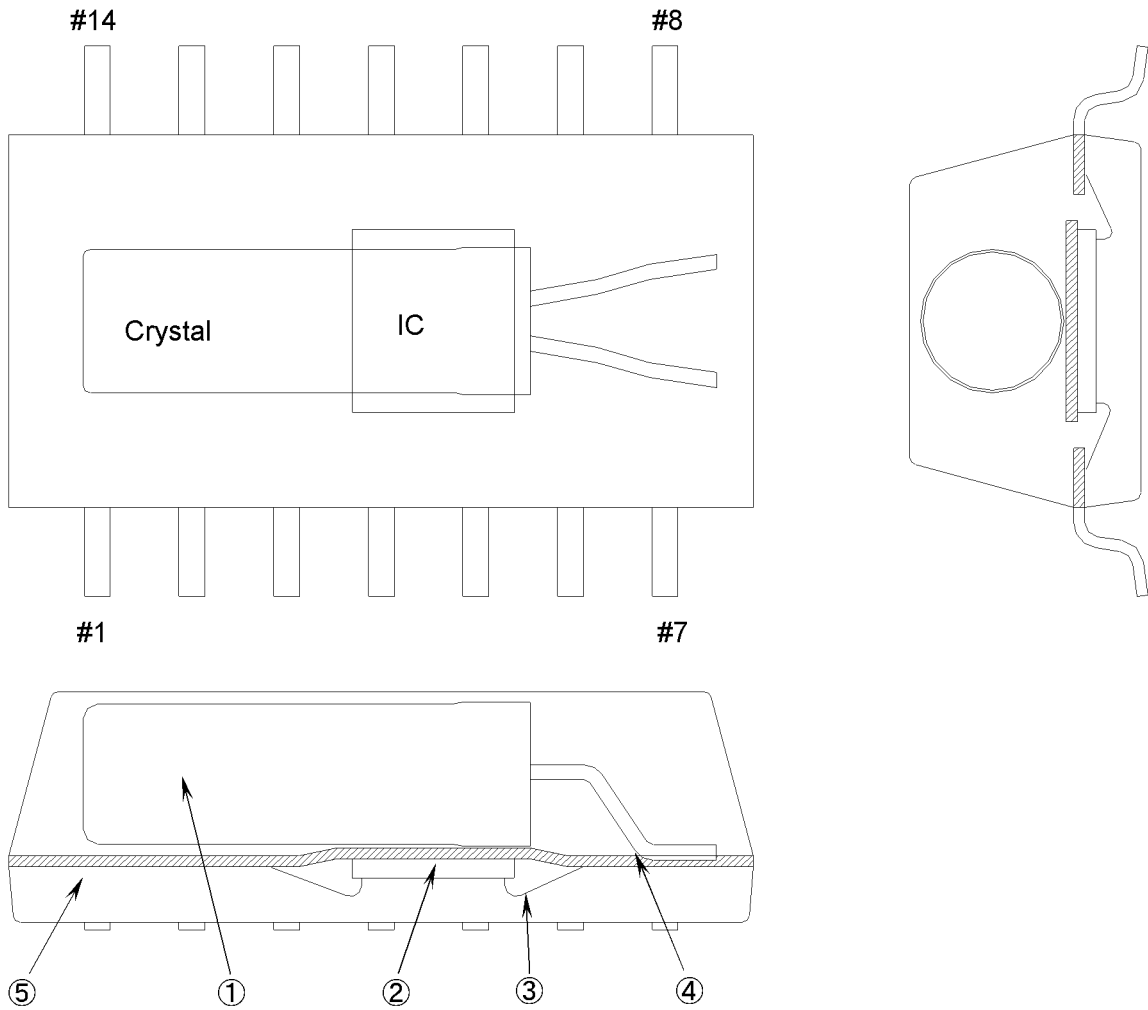
No. SOP14-RC-PbF-ATE-1

Real Time Clock Module SOP 14pin

2013.6.14

Manufacturing process chart	No.	Section In charge	Standards & Specifications	Inspection & Control Item	Inspection Instruments	Inspection methods	Record
	1	QA section	Purchasing specification Incoming Inspection standard	Appearance Dimension	Microscope	Sampling	Data Sheet
	1-1	Subcontractor	Incoming Inspection standard	Model,Quantity	Visual inspection	Sampling	Data sheet
	1-2	Subcontractor	Incoming Inspection standard	Model,Quantity, Appearance	Visual inspection	Sampling	Data sheet
	2	Subcontractor	Assemble specification	Appearance	Visual inspection	Sampling	Data sheet
	3	Subcontractor	Assemble specification	Appearance (chip/paste) Die shear strength Baking temperature,time	Microscope ,Visual inspection Pull-Gsuge Thermometer,Timer	Sampling	Data sheet
	4	Subcontractor	Assemble specification	Wire-pull strength Bonding strength U.S power Temperature,Force Appearance	Pull-tester Ball-share tester Thermometer,Gauge Dial-gauge Microscope	Sampling	Data sheet
	1-3	Subcontractor	Incoming inspection standerd	Model,Quantity	Visual inspection	Sampling	Data sheet
	5	Subcontractor	Assemble specification	Welding-power Pressure,Crystal position Appearance	Power-measure Gauge Microscope	Sampling 100% Inspection	Data sheet
	6	Subcontractor	Assemble specification	Shape of bonded wire Mould Die-temperature Curing-Temperature,Time Appearance	Surface-thermometer Thermometer,Timer X-ray Visual Inspection	Sampling 100% Inspection	Data sheet
	7	Subcontractor	Assemble specification	Belt speed, Time,Tact Plating thickness, Solder ability Appearance	Timer,Thermometer Fluorescent X-ray Microscope Visual inspection	Sampling	Data sheet
	8	Subcontractor	Assemble specification	Appearance	Visual inspection	Sampling	Data sheet
	9	Subcontractor	Assemble specification	Appearance Outer Dimention	Microscope	Sampling	Data sheet
	10	Subcontractor	Manufacturing Instruction Sheet	Electrical characteristics	Measuring equipment	100% Inspection	Data sheet
	11	Subcontractor	Manufacturing Instruction Sheet	Temperature,Time	Thermometer,Timer	Every lot	Data sheet
	12	Subcontractor	Manufacturing Instruction Sheet	Temperature,Time	Thermometer,Timer	Every lot	Data sheet
	13	Subcontractor	Manufacturing Instruction Sheet	Frequency Temperature characteristics	Measuring equipment	100% Inspection	Data sheet
	14	Subcontractor	Manufacturing Instruction Sheet	Electrical characteristics	Measuring equipment	100% Inspection	Data sheet
	15	Subcontractor	Inspection standard	Electrical characteristics Appearance	Measuring equipment Visual inspection	Sampling	Data sheet
	16	Subcontractor	Assemble specification	Tape peel strength Products direction	Peel strength tester Camera detection	Sampling 100% Inspection	Data sheet
17	Subcontractor	Assemble specification	—————	—————	—————	—————	
18	QA section	Specification sheet	Specification Appearance	—————	Every lot	—————	
19	Production control section	Manufacturing Instruction sheet Daily shipping list	Customers Type Quantity	—————	—————	—————	

RA8803SA Structure Diagram



LIST			
Name of part		Specification	
①	Crystal	Cylinder type	
	Crystal mount	Welding	
②	IC (CMOS)	Silicon	
	IC adhesive	Ag-Paste	
③	Bonding wire	Au wire	
④	Lead Frame	42 Alloy	
	Surface treatment	Inner	Ag
		Outer	Sn 100%
⑤	Transfer molding compound	Epoxy compound (Halide free)	

RELIABILITY TEST DATA

Product Name : RA8803SA

The Company evaluation condition

We evaluate environmental and mechanical characteristics by the following test condition .

No. F-R-1302-01-001EK

No.	ITEM	TEST CONDITIONS	VALUE *1		TEST Qty [n]	FAIL Qty [n]
			$\Delta f / f$ *2 [1×10^{-6}]	Electrical characteristics		
1	High temperature storage	+125 °C × 1 000 h	*3 ± 50	Satisfy specification after test	22	0
2	Low temperature storage	-55 °C × 1 000 h	*3 ± 10		22	0
3	High temperature bias	+85 °C × 5.5 V × 1 000 h	*3 ± 20		22	0
4	Low temperature bias	-40 °C × 5.5 V × 1 000 h	*3 ± 10		22	0
5	Temperature humidity bias	+85 °C × 85 %RH × 5.5 V × 1 000 h	*3 ± 20		22	0
6	Temperature cycle	-40 °C ↔ +85 °C 30 min at each temp. 1000 cycles	*3 ± 10		22	0
7	Resistance to soldering heat	For convention reflow soldering furnace (3 times) Follow JEDEC J-STD-020D.1	± 8		22	0
8	Drop	Free drop from 750 mm height on a hard wooden board for 3 times (Board is thickness more than 30 mm)	± 5		22	0
9	Vibration	10 Hz to 55 Hz amplitude 0.75 mm 55 Hz to 500 Hz acceleration 98 m/s ² 10 Hz → 500 Hz → 10 Hz 15 min/cycle 6 h (2 h × 3 directions)	± 5		22	0
10	Solderability	Dip termination into solder bath at +235 °C ± 5 °C for 5 s (Using Rosin Flux)	Termination must be 95 % covered with fresh solder		11	0

Notes

*1 Each test done independently.

*2 Measuring 2 h to 24 h later leaving in room temperature after each test.

*3 Pre-conditions (Dry +125°Cx24h→ high temp & humidity +85°Cx85%RHx168h→Reflow 3times) should be performed before each tests. Pre conditionings Initial value shall be after 24 h at room temperature.

Product Name : RA8803SA

Frequency Shift Rate $\Delta f / f$

No. F-R-1302-01-002EK

