General Description

The YQ1S310 is a high-performance, low-skew and low-power clock buffer that distributes 10 clock outputs from one out of three inputs. The three inputs include primary/ secondary differential/single-end inputs and crystal inputs. The YQ1S310 is suitable for a variety of mobile and wired infrastructure, data communications, computing, low-power medical imaging, and portable test and measurement applications. When the input is an illegal voltage-level, the input should be in a definite state. The core supply operates on 2.5-V or 3.3-V, and outputs supply operates on 1.5-V, 1.8-V, 2.5-V or 3.3-V. Pins-programming allows easy configuration of YQ1S310. The total additive jitter is 25fs-rms(typical). YQ1S310 is available in 32-pin 5mm x 5mm QFN package.

Applications

➢ **Mobile and Wired Infrastructure**
➢ **Network and Data Communications**
➢ **Medical Imaging**
➢ **Portable Test and Measurement**
➢ **High-end Audio and Video**

Features

▪ **2.5V or 3.3V core supply and flexible 1.5V, 1.8V, 2.5V, 3.3V outputs supply**
▪ **Ultra-low noise floor(-169dBc/Hz) crystal oscillator buffer**
▪ **Additive jitter is 25fs-rms (Typical)**
▪ **Device inputs include primary, secondary, and crystal inputs, and manually selectable (through pins) using the MUX. The primary and secondary inputs can accept LVPECL, LVDS, HCSL, SSTL or LVCMOS signal.**
  – **Crystal Frequency from 8MHz to 100MHz**
  – **Differential and single-end inputs operate up to 200MHz**
▪ **High-Performance 1:10 LVCMOS Clock Buffers.**
  – **LVCMOS outputs operate up to 200MH**
  – **Output skew is 30ps (Typical)**
  – **Total propagation delay is 2ns (Typical)**
  – **Synchronous and glitch-free output enable is available**
▪ **Available in 32-pin 5mm x 5mm QFN package**
▪ **Can overdrive crystal input with LVCMOS signal up to 100MHz**
▪ **-40° to +85°C industrial temperature operation applications**

Functional Block Diagram
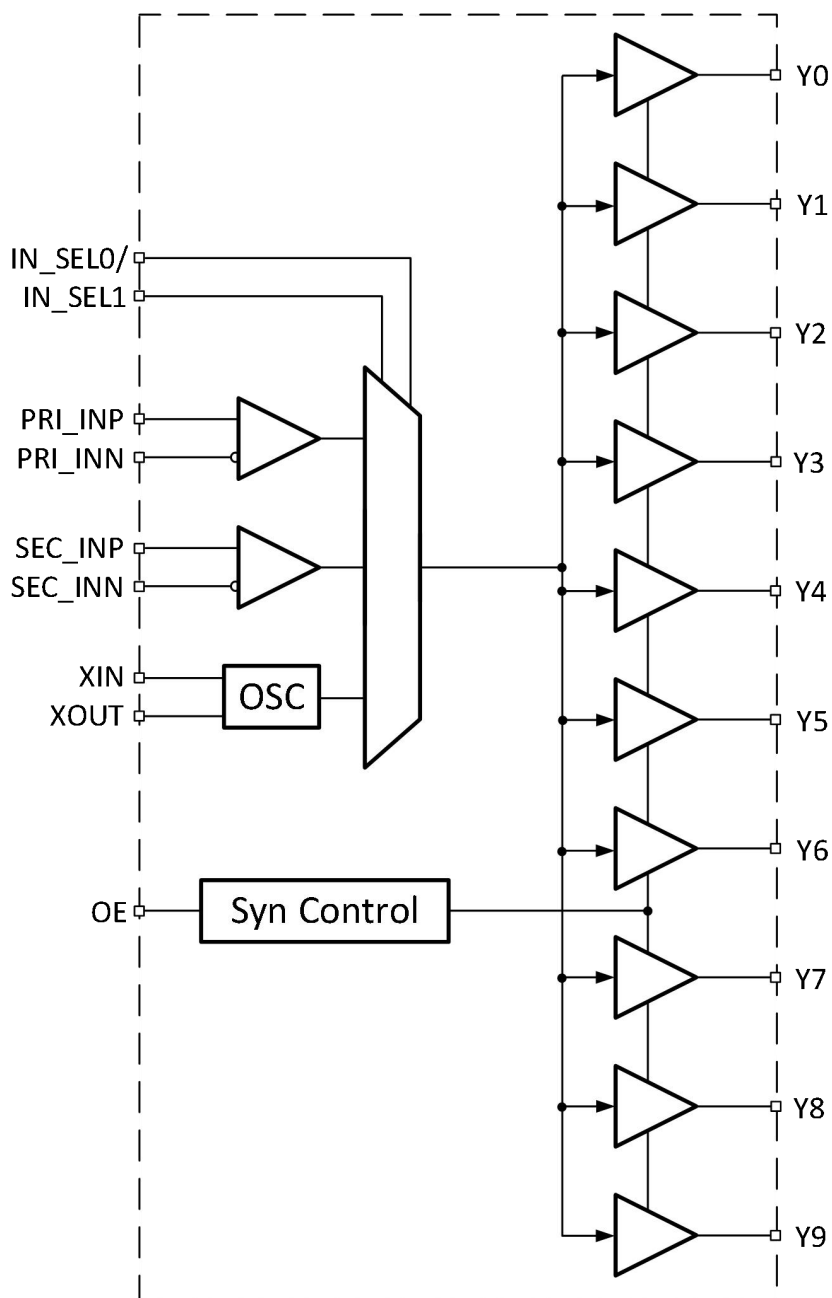
Pin Configuration
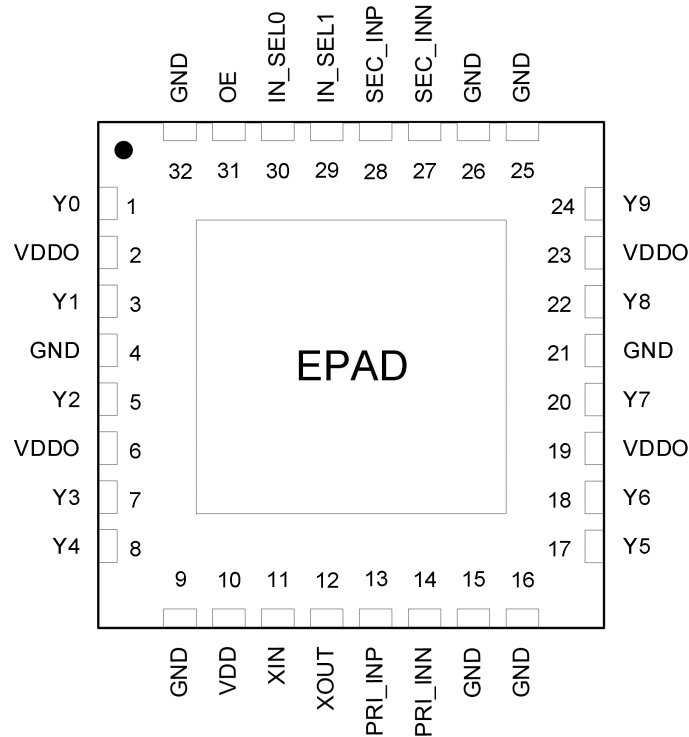
32-pin 5mm x 5mm QFN (Top View)

Pin Functions

Number	Name	Type	Description
4, 9, 15, 16, 21, 25, 26, 32	GND	Ground	Ground
10	VDD	Power	DC power supply. Connect to 2.5V to 3.3V
2, 6, 19, 23	VDDO	Power	I/O power supply. Connect to 1.5V, 1.8V, 2.5V, 3.3V
30	IN_SEL0	Input	Input-clock selection (pulldown of 150 kΩ)
29	IN_SEL1	Input	Input-clock selection (pulldown of 150 kΩ)
31	OE	Input	LVCMOS output enable (pulldown of 150 kΩ)
13	PRI_INP	Input	Non-inverting differential or single-ended primary reference input (pulldown of 150 kΩ)
14	PRI_INN	Input	Inverting differential primary reference input, internally biased to Vdd / 2 (pullup or pulldown of 150 kΩ)
28	SEC_INP	Input	Non-inverting differential or single-ended primary reference input (pulldown of 150 kΩ)
27	SEC_INN	Input	Inverting differential primary reference input, internally biased to Vdd / 2 (pullup or pulldown of 150 kΩ)
11	XIN	Input	Crystal-oscillator input or XTAL bypass mode
12	XOUT	Input	Crystal-oscillator output
1	Y0	Output	LVCMOS output 0
3	Y1	Output	LVCMOS output 1
5	Y2	Output	LVCMOS output 2

7	Y3	Output	LVCMOS output 3
8	Y4	Output	LVCMOS output 4
17	Y5	Output	LVCMOS output 5
18	Y6	Output	LVCMOS output 6
20	Y7	Output	LVCMOS output 7
22	Y8	Output	LVCMOS output 8
24	Y9	Output	LVCMOS output 9

Table 1. Input Selection

IN_SEL1	IN_SEL0	INPUT CHOSEN
0	0	PRI_INP/PRI_INN
0	1	SEC_INP/SEC_INN
1	x	XTAL or overdrive

Table 2. INPUT/OUTPUT OPERATION [1]

INPUT STATE	OUTPUT STATE
PRI_INx, SEC_INx open	Logic LOW
PRI_INP, SEC_INP = HIGH, PRI_INN, SEC_INN = LOW	Logic HIGH
PRI_INP, SEC_INP = LOW, PRI_INN, SEC_INN = HIGH	Logic LOW

(1) Device must have switching edge to obtain output states.

Specifications

Absolute Maximum Ratings

Item	Rating
Supply Voltage,VDD	3.465V
Inputs CLKIN/1G	-0.3V ~ VDD+ 0.3V
Package Thermal Impedance, Θ_{JA}	42°C/W (0 mps)
Package Thermal Impedance, Θ_{JC}	41.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	4000V
Junction Temperature	125°C

Electrical Characteristics

(VDD = 3.3V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage for supporting 3.3V outputs		3.135	3.3	3.465	V
V_{IH}	High-level input voltage		0.7*VDD		1.05*VDD	
V_{IL}	Low-level output voltage		GND		0.3*VDD	
V_{OH}	High-level output voltage	I_{OH} = −8 mA	2.5			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	
I_{DD}	Supply Current	100MHz, CL=5pF		50		mA

(VDD = 2.5V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage for supporting 2.5V outputs.		2.375	2.5	2.625	V
V_{IH}	High-level input voltage		0.7*VDD		1.05*VDD	
V_{IL}	Low-level output voltage		GND		0.3*VDD	
V_{OH}	High-level output voltage	I_{OH} = −8 mA	1.9			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	
I_{DD}	Supply Current	100MHz		35		mA

(VDD = 1.8V ± 5%, TA = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDD	Power supply voltage for supporting 1.8V outputs.		1.71	1.8	1.89	V
V_{IH}	High-level input voltage		0.7*VDD		1.05*VDD	
V_{IL}	Low-level output voltage		GND		0.3*VDD	
V_{OH}	High-level output voltage	I_{OH} = −8 mA	1.2			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.5	
I_{DD}	Supply Current	100MHz		25		mA

AC Timing Characteristics

(VDD = 3.3V ± 5%, TA = -40°C to +85°C)

INPUT CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
F_{clkin}	Input Frequency	VDD = 3.3V	10^{-6}		250	MHz
		VDD = 2.5V	10^{-6}		200	MHz
Single-Ended DC Characteristic						
VIH	Input high voltage		2		VDD+0.3	V
VIL	Input low voltage		-0.3		1.3	V
VINH_SEL	IN_SEL high voltage		2		VDD+0.3	V
VINL_SEL	IN_SEL low voltage		-0.3		1.3	V
Differential DC Characteristic						
VID	Differential input voltage swing		0.15		1.3	V
VCMD	input common mode voltage		0.5		VDD – 0.85	V
T_{IDC}	Input Duty Cycle	Duty Cycle	45		55	%

LVCMOS OUTPUT CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Frequency	Output frequency limit	10^{-6}		200	MHz
T_{ODC}	Output Duty Cycle	Duty Cycle	45		55	%
T_R	Rise Times	20% to 80%		350	1000	ps
T_F	Fall Times	80% to 20%		350	1000	ps
T_{jitter}	Additive Jitter	156.25MHz, 12kHz to 20MHz, 3.3V, OSC Differential input		28	35	fs
		156.25MHz, 12kHz to 20MHz, 2.5V, OSC Differential input		58	80	fs
T_{sk_o}	Output to output skew				50	ps
T_{pd}	propagation delay			2		ns

Typical Phase Noise with 156.25MHz Crystal Input at 3.3-V supply
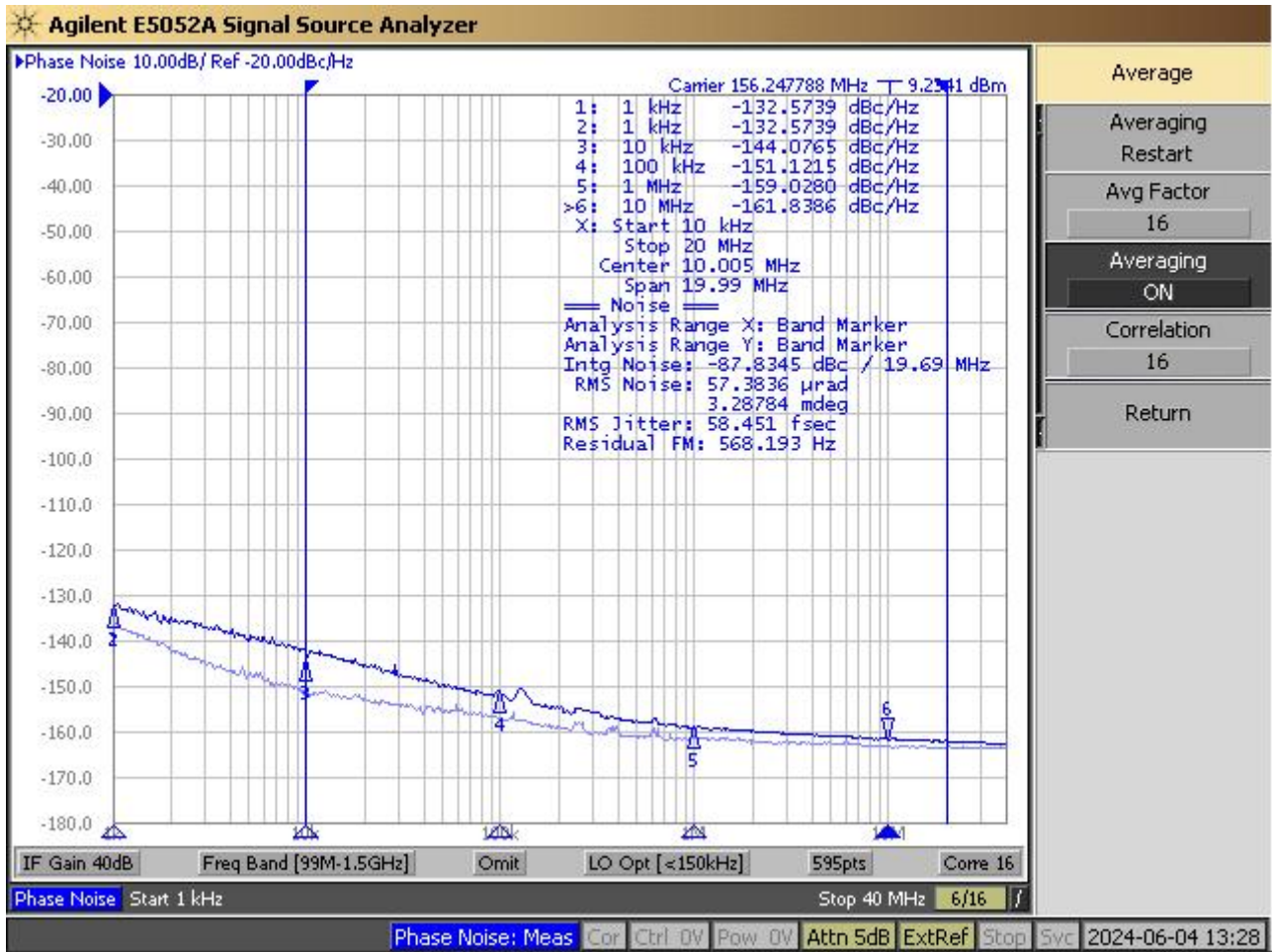
Detailed Description

Overview

The YQ1S310 is a 10-output clock fan out buffer with low additive jitter that can operate up to 250 MHz. The device is offered in a QFN55-32 package. For best signal integrity, it is important to match the characteristic impedance of the YQ1S310's output driver with that of the transmission line.
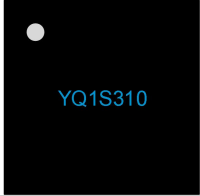
Output Enable

Pulling OE to LOW, forces the outputs to the high-impedance state after the next falling edge of the input signal. The outputs remain in the high-impedance state as long as OE is LOW.

Parameter Measurement Information
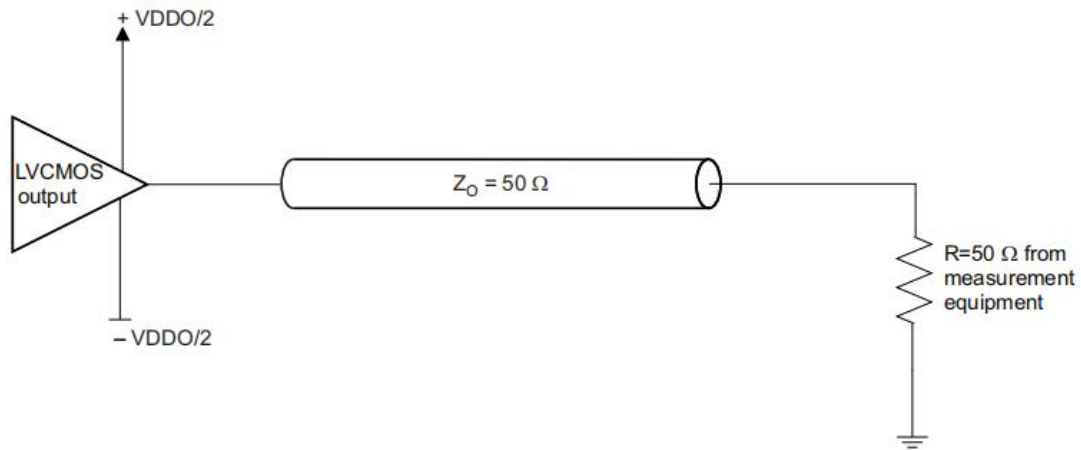
LVCMOS Output DC Configuration; Test Load Circuit
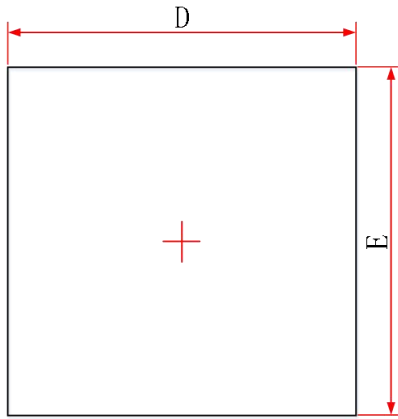
Order Information

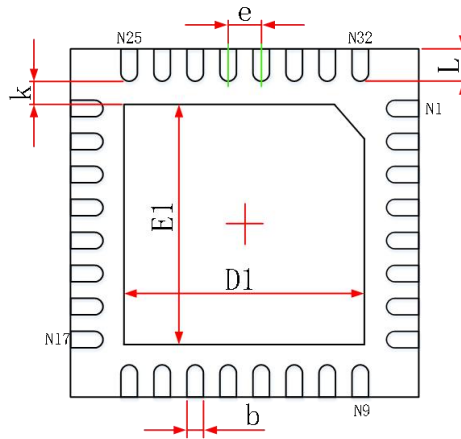| Part No.	Package	Mark	Tape and Reel Information
YQ1S310	QFN 5mmX5mm-32L	YQ1S310	xxxxpcs/Reel

Package Outline

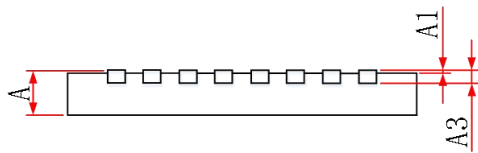### QFN 5mmX5mm-32L

Quad Flat No-Lead Package, 32 leads.

Body width 5mm, body length 5mm, body thickness 0.8mm, lead pitch 0.5mm.

Top View

Bottom View

Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

Revision History

No	Date	Description
V1.0	202308	First release