「日・英の記述に相違がある場合は、日本語を優先とする」

SEIKO EPSON CORPORATION HIROOKA OFFICE

RECIPIENT

SPECIFICATIONS

MODEL : RTC-9825B SA

SPEC. No. : Q12-250-1B2

DATE: Mar. 28. 2013

SEIKO EPSON CORPORATION

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Update History

Date	Page	Item	Current	Update
Mar.28,2013	New Issue			

SPECIFICATIONS

1. Application

1) This document is applicable to the crystal unit that are delivered to
SEIKO EPSON CORPORATION HIROOKA OFFICE from Seiko Epson Corp.
2) This product complies with RoHS Directive.
3) You are requested, if applicable, to obtain all necessary licenses for the export of this product(s)
(including any technical information furnished, if any) under Foreign Exchange and Foreign Trade Law.
You are requested not to export this product(s) in order to use it for development and/or manufacture of weapons of mass destruction or for other military purposes. Exporting this product(s) in order to make it available to any third party who uses or may use this product(s) for such purposes are also prohibited.
4) This product listed here is designed as components or parts for electronics equipment in general consumer use.
We do not expect that any of these products would be incorporated or otherwise used as a component or part for the equipment, which requires an systems, and medical equipment, the functional purpose of which is to keep extra high reliability, such as satellite, rocket and other space life.

2. Model

The model is RTC-9825B SA.

3. Packing

It is subject to the packing standard of Seiko Epson Corp.

4. Warranty

Defective parts which are originated by us are replaced free of charge in case defects are found within 12 months after delivery.

5. Amendment and abolishment

Amendment and/or abolishment of this specification are subject to the agreement between both parties.

6. Contents

7. Production Country

Crystal Unit

Country	Plant	Addles
Japan	INA plant	8548 Nakaminowa,Minowa-machi,Kamiina-gun,Nagano,Japan
China	ETSZ	No.144, Hua Shan Road, Suzhou New District, Suzhou, Jiangsu China
Malaysia	EPMY	Lot 1,Jalan Persiaran Industri, Taman Perindustrian Sri Damansara, Sungai Buloh,52200 Kuala Lumpur

RTC

Country	Plant	Addles
Japan	KATOH Electric Co., Ltd.	6392 Kamiyoshida,Fujiyoshida-shi,Yamanashi,Japan
Japan	AOI ELECTRONICS CO/, LTD.	455-1 Takamatsu-shi,Kagawa,Japan

Crystal chip (Wafer)

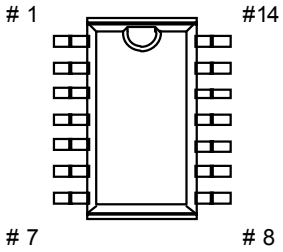
Country	Plant	Addles
Japan	MIYAZAKI plant	1860, Hei, Imaizumi, Kiyotake-cho, Miyazaki-shi, Miyazaki 889-1602, Japan
Japan	AKITA EPSON CORP.(AEC)	1, Dannoue, Iwasaki-Aza, Yuzawa-City, Akita-Ken 012-0801 Japan

I C Chip

Country	Plant	Addles
Japan	Fujimi Plant	281 Fujimi,Fujimi-chou,Suwa-gun,Nagano,Japan

[1]SA Terminal connections

RTC – 9825B SA



1. N.C.
2. DO
3. DI
4. CLK
5. CE
6. IRQ
7. GND
14. V_{DD}
13. FRST
12. VI5
11. RST
10. VEX
9. EXO
8. V_{DD2}

SOP - 14 pin

Custom logic + EEPROM + voltage detection (2 circuits) + FRST

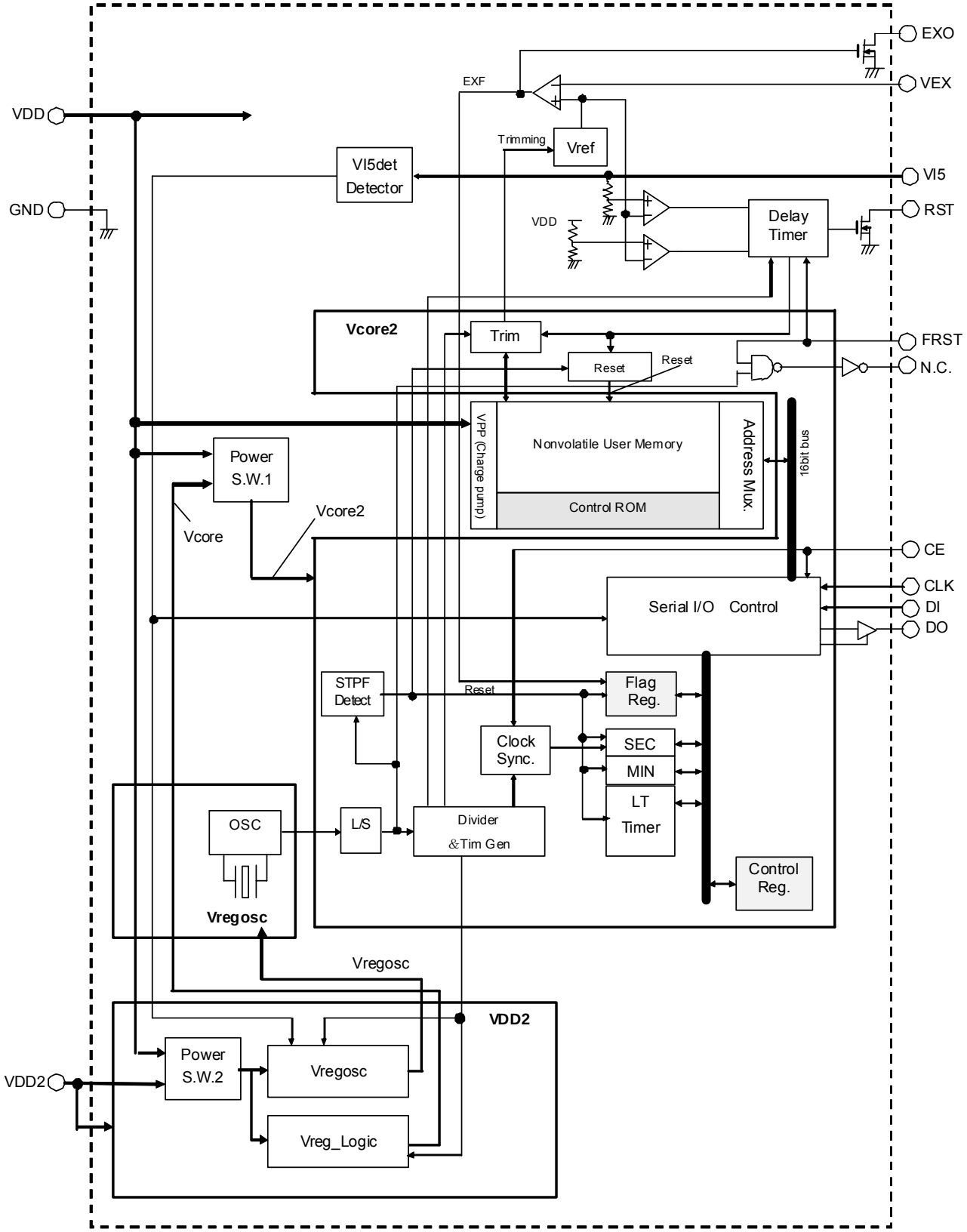
No.	Name	I/O	Comments	No.	Name	I/O	Comments
1	N.C.	O	Test output*1	14	VDD		Power supply
2	DO	O	Serial data output	13	FRST	I	Forced reset
3	DI	I	Serial data input	12	VI5	AIN	Voltage detection at 5 V
4	CLK	I	Serial clock input	11	RST	O.D.	Reset output
5	CE	I	Serial chip enabled	10	VEX	AIN	Input pin for detecting external voltage
6	IRQ	N.C.	It is not connected inside	9	EXO	O.D.	Output pin for detecting external voltage
7	GND		Power Supply	8	VDD2		Backup power supply

*1 Be sure to leave N.C. pin Open (unconnected).

*2 V_{DD2} is in an open state, and RTC can work.

*3 Be sure to connect a filter capacitor of at least 0.1 μF near V_{DD}–GND and V_{DD2}–GND.
Can replace it with RTC-9825B SA in a circuitry same as RTC9825SA substituting filter capacitor between VDD2-GND with a large-capacity condenser for backup.

[2] Block diagram



∗1. Terminate the input (Do not leave them in the Hi-z state.)
∗2. Be sure to keep free N.C terminal and IRQ terminal. (unconnected)
∗3. Higher voltage either of VDD or Vcore is supplied to Vcore2 through "Power S.W.1"
∗4. Higher voltage either of V_{DD} or V_{DD2} is supplied to Vreg through “Power S.W.2”.

[3] Absolute maximum ratings

GND=0 V

Item	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	–	-0.3 to 4.5	V
	V_{DD2}	–	-0.3 to 6.0	V
Input voltage	V_{IN}	Input pin	GND-0.3 to V_{DD}+0.3	V
	V_{AIN}	Analog input pin	-0.3 to 6.0	V
Output voltage	V_{OUT}	EXO,DO	GND-0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	–	-55 ~ +125	°C

[4] Operating range

Item	Symbol	Condition	Range	Unit
Operation power supply voltage	V_{DD}	When using NVMEMORY or communicating	2.7 to 3.6	V
RTC power supply voltage	V_{DD2}		1.8 to 5.5	V
Timekeeper voltage range	V_{DD2T}	Power voltage that is able to do continuous time counting with RTC after starting oscillation (1.8V≤V_{DD2}) even if makes dropping of V_{DD2}	1.4 to 5.5	V
Operation temperature	T_{OPR}	No condensation	-40 to +85	°C

[5] Oscillation characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	fo	Ta=+25 °C, V_{DD2} or V_{DD}=3.0 V		32.768		kHz
Frequency precision	ΔFout/fo	Ta=+25 °C, V_{DD2} or V_{DD}=3.0 V	-1000		+1000	$\times 10^{-6}$
Oscillation start time	t_{STA}	Ta=+25 °C, V_{DD2}=1.8 V to 5.5 V or V_{DD}=2.7 V to 3.6 V,FRST=Low			1	s
		Ta=±0 °C to 40 °C V_{DD2}=2.2 V to 5.5 V or V_{DD}=2.7 V to 3.6 V,FRST=Low			0.425	s
Frequency / temperature characterictics	T_f	Ta=-20 °C to +70 °C, standard is +25 °C	-120		+10	$\times 10^{-6}$
Frequency / voltage characteristics	f / V	Ta=+25 °C, V_{DD2}=1.8 V to 5.5 V or V_{DD}=2.7 V to 3.6 V	-2		+2	$\times 10^{-6}$/V
Aging	fa	Ta=+25 °C	-5		+5	$\times 10^{-6}$/Year

[6] DC characteristics

If not specifically indicated: GND = 0V, VDD = 2.7 V to 3.6 V, VDD2 = 1.8 V to 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{DD} current consumption	I_{DD1}	V_{DD} =3.0 ,VI5=5.0 V		30	100	μA
	I_{DD2}	VDD=3.0V , VI5=5.0V Inrush current at the time of the VDD power-on.		3	10	μA
V_{DD2} current consumption	I_{BK1}	V_{DD}=VI5=0 V, V_{DD2}=5.5 V , FRST=Low , Ta=-20 °C to +70 °C		0.45	0.6	μA
	I_{BK2}	VDD=VI5=0V , VDD2=5.5V , FRST=Low Ta=-20°C to +70°C Inrush current at the time of the VDD2 power-on		3	10	μA
	I_{BK3}	V_{DD}=3.0V , VI5=5.0V, V_{DD2}=5.5V , FRST=Low Ta=-20°C to +70°C		0.55	3	μA
Input voltage	V_{IH}	CE,CLK,DI,FRST	0.8V_{DD}		V_{DD}	V
	V_{IL}	CE,CLK,DI,FRST	0		0.2V_{DD}	V
VI5 Input voltage	VI5det	VI5	0.30		0.80	V
Input leakage current	ILK	CE,CLK,DI VIN= V_{DD} or GND	-0.5		0.5	μA
Output leakage current	IOZ	DO VOUT= V_{DD} or GND	-0.5		0.5	μA
DO output voltage	V_{OH2}	IOH= -1 mA	V_{DD}-0.4			V
	V_{OL2}	IOL= 1 mA			GND+0.4	V
O.D. output voltage	V_{OL3}	EXO IOL= 1 mA			GND+0.4	V
O.D. output voltage	V_{OL4}	RST IOL= 2 mA			GND+0.4	V

* Typ. : Only reference value.

[7] AC characteristics

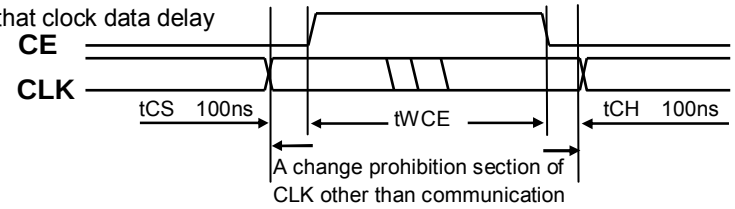
If not specifically indicated: GND = 0 V, VDD = 2.7 V to 3.6 V, VDD2 = 1.8 V to 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK clock cycle	t_{CLK}		750			ns
CLK H pulse width	t_{WH}		350			ns
CLK L pulse width	t_{WL}		350			ns
CE setup time	t_{CS}		100			ns
CE hold time	t_{CH}		100			ns
CE recovery time	t_{CR}		100			ns
CE enable time	t_{WCE}		-		1	s
Write data setup time	t_{DS}		150			ns
Write data hold time	t_{DH}		150			ns
Read data delay time	t_{RD}	CL=50 pF			300	ns
DO output mode switching time	t_{ZR}				20	ns
DO output disable time	t_{RZ}	CL=50 pF,RL=10 kΩ			20	ns
DI/DO conflict circuit time	t_{ZZ}		0			ns
Ready setup time	t_{RDY}		20			ns
Input rise/fall time	t_r/t_f	20% to 80% of VDD			10	ns
Time update Busy*	t_{carry}	X'tal=32.768 kHz			7.8125	ms

The Busy signal is 2 kinds OR output of "Writing to EEPROM" and " During the time updating of the Long timer".
Accordingly, there is the possibility that the longest Busy signal becomes 11.8125 ms.

Note: About level-change of signals except data communications.

When a level of each communication line changes besides serial data communication, there is a case to produce communication error. Don't change the level of CLK, when CE is HI and the before and after 100ns.
By a case, data-hold function acts, and there is the case that clock data delay



[8] VEX voltage detection characteristics

If not specifically indicated: GND = 0 V, V_{DD}=2.7 V ~ 3.6V, VI5 = 4.5 V to 5.5 V, Ta = -20 °C to +70 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXO output delay time	t_{HX}				2	μs
Reset LOW time	t_{LDL}				1.5	μs
Voltage detection	V_{DT3}	VEX pin*2		2.0		V
	V_{DT3N}	*1 *2When initial power-on or when level of V_{DD},VI5 are not decided	1.75		2.1	
Voltage detection precision		Ta=-40 °C to +85 °C	-4		+4	%
Hysteresis voltage	V_{HIS}		30	50	100	mV
EXO Low Active lower voltage	V_{ACT}	IOL=1 mA , VOL=0.4 V		1.4		V
Unresponsive time					1.5	μs

*1. When starts up V_{DD}, VI5 and V_{DD2} from 0V (in case trimming data of reference voltage for voltage detection circuit is not loaded to register)

*2. Detection voltage in case of falling voltage.

[9] Reset voltage detection characteristics

If not specifically indicated: GND = 0 V, VI5 = 4.5 V to 5.5 V, Ta = -20 °C to +70 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset delay time	t_{HDL}	*2*5when oscillating V_{DD2}=1.8 V to 5.5 V	94		125	ms
	t_{HDLN}	*3*5 When initial power-on Ta=±0 °C to +40 °C V_{DD2}=2.2 V to 5.5 V,FRST=Low	94		550	ms
V_{DD} voltage detection	VRST	*5 For 3V	2.4	2.5	2.6	V
	VRSTN	*4*5 When up initial power-on	2.15		2.60	V
VI5 voltage detection	VI5	*5 For 5V	4.0	4.2	4.4	V
	VI5N	*4*5 When initial power-on	3.60		4.40	V
Hysteresis voltage	V_{HIS}		30	50	100	mV
RST Low Active lower voltage	V_{ACT}	IOL=1 mA , VOL=0.4 V		1.4		V
Reset LOW time	t_{LDL1}	Input the following pulse: VDD = 3.0 V to 2.0 V			4	μs
Unresponsive time					2	μs
Reset LOW time	t_{LDL2}	Input the following pulse: VI5 = 4.5 V to 3.5 V			1	μs
Unresponsive time					1	μs

*2. *3. Please refer to item [13] external reset circuit.

*4. When starts up V_{DD}, VI5 and V_{DD2} form 0V (in case trimming data of reference voltage for voltage detection circuit is not loaded to register)

*5.Detection voltage in case of falling voltage.

[10] Nonvolatile Memory characteristics

If not specifically indicated: GND=0 V, V_{DD}=2.7 V ~ 3.6 V,VI5=0.3V ~ 0.8V over,V_{DD2}=1.8 V ~ 5.5 V, Ta=-20°C ~ 70 °C

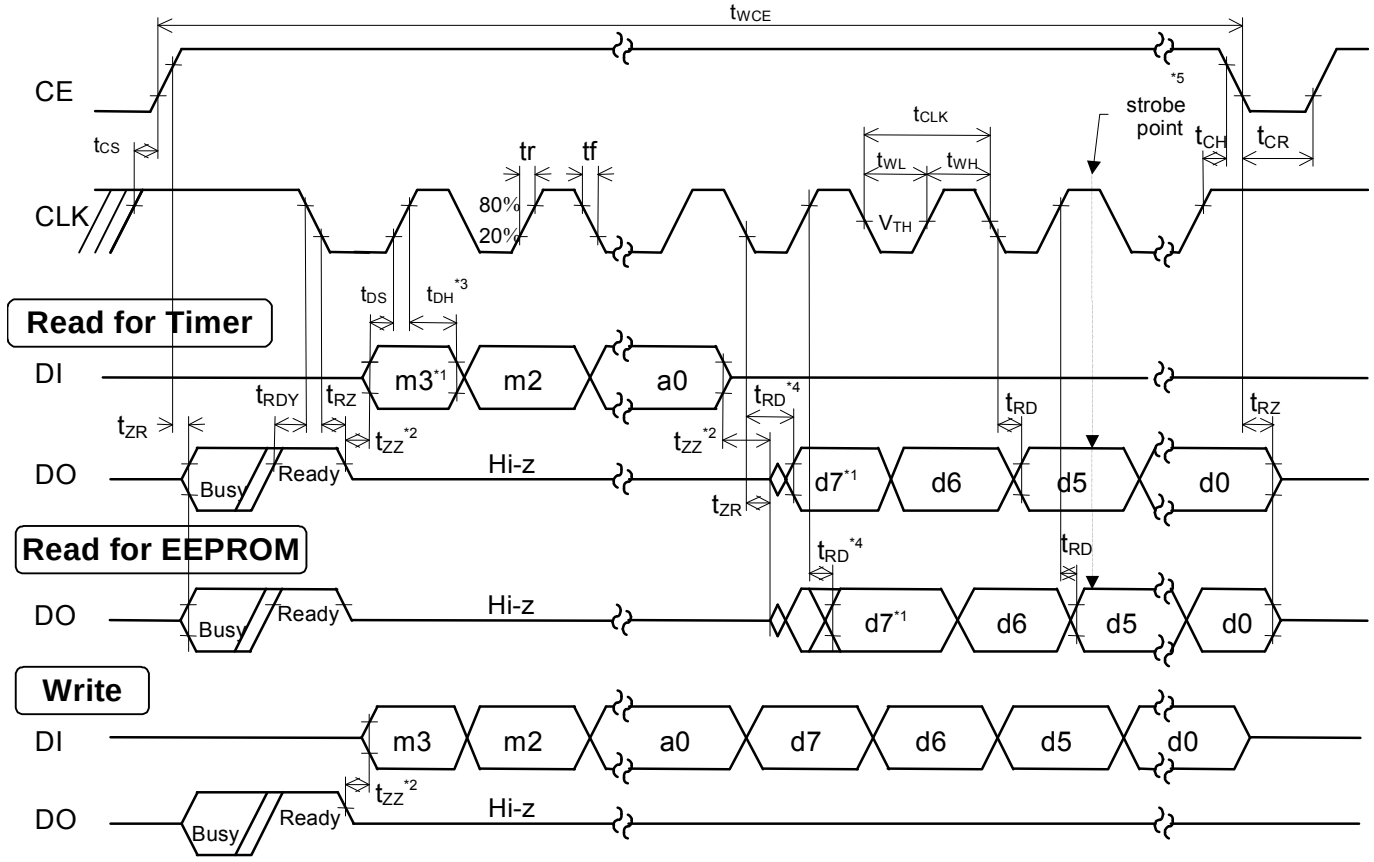
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Memory structure			4 kbit(254×16 bit)			
Program/Erase Cycle			100000			cycles
Current consumption	I_{DD3}	Write to NVMEMORY			1.5	mA
	I_{DD4}	Read to NVMEMORY			0.4	mA
Access time	t_{WNV}		1.9		2.2	ms

* After writes to the nonvolatile memory are completed, be sure to wait at least T_{WNV} before turning OFF the power.

[11] Timing chart

11.1 Read & Write Timing (for Custom mode)

During data transfer, carry operations are put on hold, and a Busy signal (0: Busy / 1: Ready) is output from DO immediately after communication starts (CE = HIGH). When the pin is in the ready state, communication is possible. When the pin is in the busy state, a time up date or write to nonvolatile memory are being performed. If this occurs, wait until the pin goes into the ready state, or terminate communication momentarily (CE = LOW) and restart after waiting for a fixed period. If data is transferred while the pin is in the busy state, data cannot be guaranteed. The Busy signal goes into the Hi-z state at the first falling edge of CLK.



∗1. Address and data width differ for RTC mode and Nonvolatile Memory mode.

∗2. When using a wired OR for DI and DO signals, allocate time (tzz) so that bus conflict is avoided.

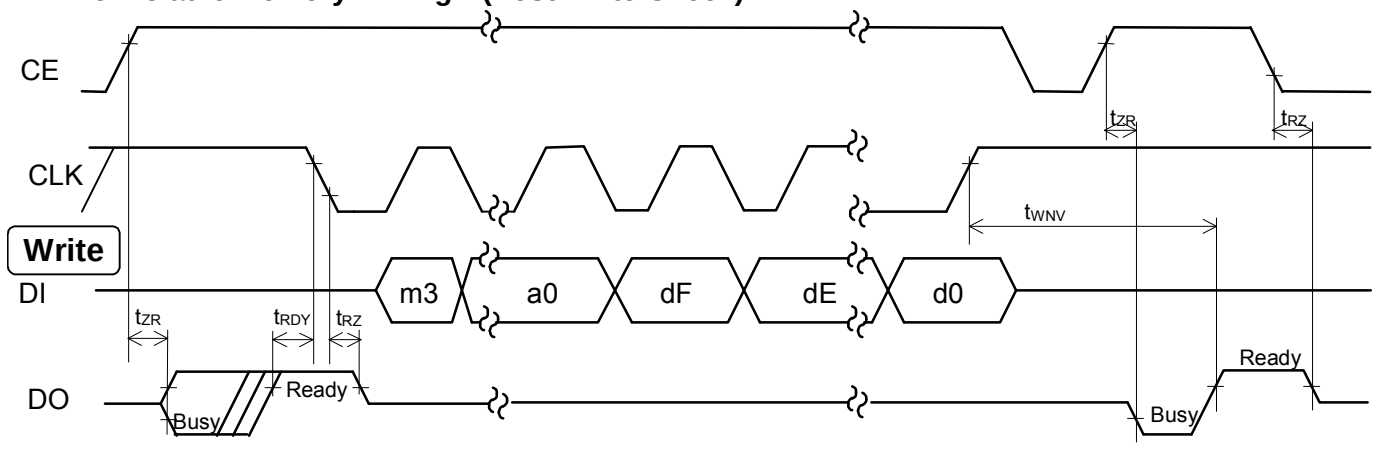
∗3. DI data “latches” to the positive edge.

∗4. DO data is output to the negative edge in Custom mode, and the positive edge in EEPROM mode. By setting the strobe point immediately before*5 the negative edge.

∗5. Do not access while RST = “L”.

∗6. When initial power is input and after falling voltage, register is unstable condition, therefore Ready signal is not output as the case may be. Please confirm Busy signal after input power and starting oscillation, access in disregard of Busy signal if Busy signal of over 11.9ms is output and try to do “0” clear of TEST bit. After that, please surely initialize all timer register. Access to EEROM concerned, please refer to item [17].

11.2 Nonvolatile Memory Timing (Post Write Check)

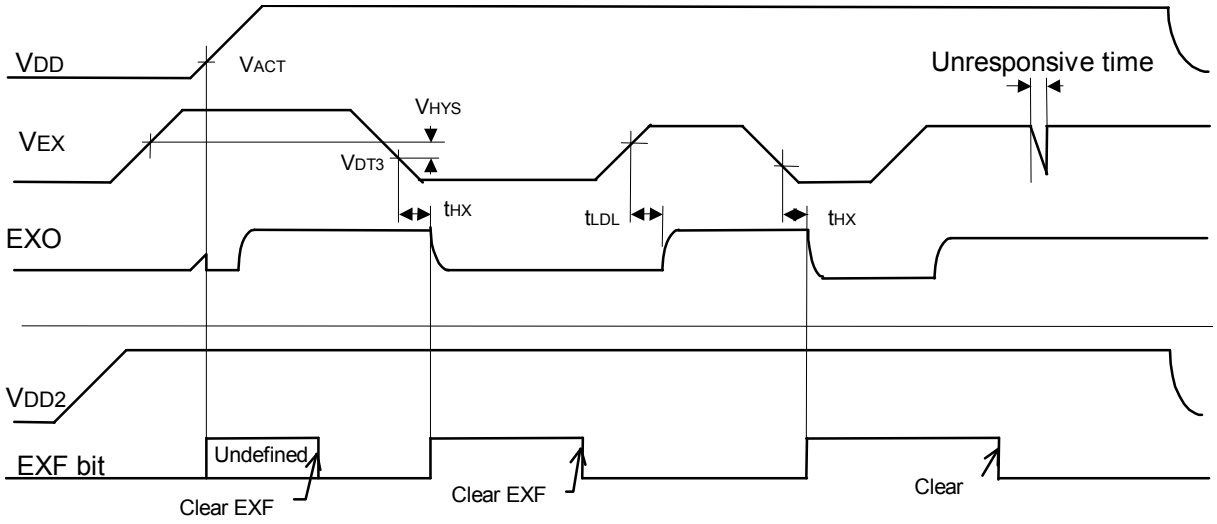


[12] External voltage detection circuit

Circuit to detect voltage that is input to VEX terminal. Output detected result to EXO terminal, and control EXF flag. If the voltage input to VEX terminal becomes higher than VDT3-VHYS, EXO terminal becomes to Hi-z. EXF flag is not changed. If the voltage input to VEX terminal becomes lower than VDT3, EXO terminal output Low. In this case, EXF flag becomes to"1". EXF flag keeps "1" until "0" has written.

Outer voltage detecting circuit works when meet all the following conditions.

1) V_{DD}=2.7 V to 3.6V or V_{DD2}=1.8V to 5.5V
2) In case oscillation circuit is worked and when 32kHz clock is propagated to internal circuit.

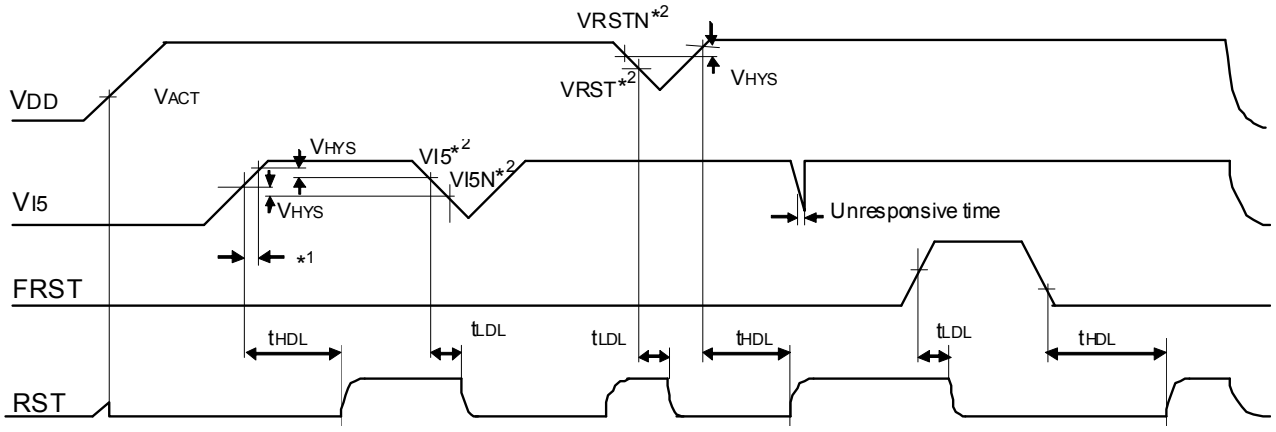


[13] External reset circuit (RST Output control function)

Detect voltage level for both V_{DD} and VI5, and control RST output. If V_{DD} voltage becomes more than VRST(VRSTN) and VI5 voltage becomes more than VI5(VI5N), RST output changes over from Low output to Hi-z after reset delay time (tHDL). And if makes FRST terminal input (forced reset input) to High when V_{DD} voltage is more than VRST and VI5 voltage is more than VI5, RST output changes over to Low output. Then if returns FRST terminal input to Low, it becomes to Hi-z after reset delay time (tHDL).

External reset circuit works if meet the following condition.

1) V_{DD}=2.7 V to 3.6V
2) VI5=4.5 V to 5.5V
3) In case oscillation circuit is worked and when 32kHz clock is propagated to internal circuit.



∗1 If level of V_{DD} and VI5 is decided, trimming of detecting voltage is loaded and detecting voltage (VRST,VI5) is fixed.
If level of V_{DD} or VI5 is uncertainly condition, an initial value is set (VRSTN,VI5N).
(Please refer to Item [14] IC Internal reset function).
If start up VI5 to voltage between 0V and [VI5N to VI5] when detecting voltage in RTC is VI5N≤VI5, or if start up V_{DD} voltage to voltage between 0V and [VRSTN to VRST] when detecting voltage in RTC is VRSTN≤VRST, voltage detecting operation may be looped between VI5N and VI5 or between VRSTN and VRST.
(In this case, hysteresis voltage VHYS in nominal measurement cannot be confirmed as the case may be)
By making starting up time of V_{DD} power and VI5 shorter than time from level decision of V_{DD} and VI5 to start load of trimming data [45ms to 62.5ms], it is able to avoid the above loop operation.
Detecting voltage to shut down power after applying V_{DD} power more than 2.60V, VI5 power more than 4.40V and after loading trimming data becomes to s VRST and VI5.

∗2 In the drawing, it is explained with VI5N≤VI5, VRSTN≥VRST, it is VI5N≤VI5, VRSTN≥VRST due to individual difference as the case may be.

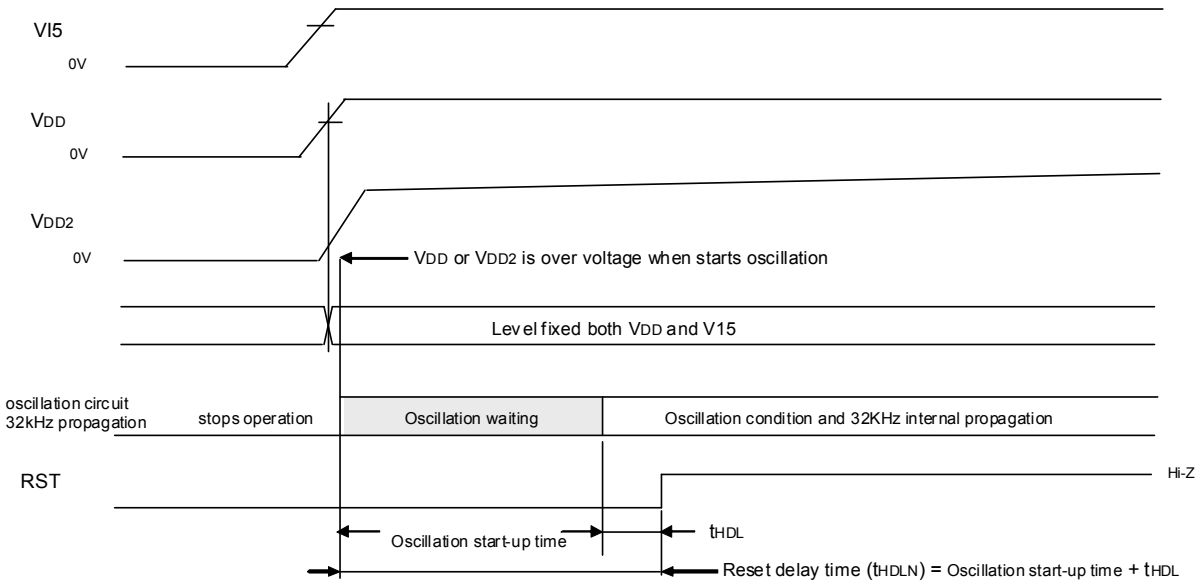
Reset delay time (tHDL) of external reset circuit is made up using divided signal from 32kHz oscillation circuit. Therefore, reset delay time is different between when start oscillation (V_{DD} from 0V or when input V_{DD2}) and when work oscillation.
Reset delay time when start oscillation is the following value.

- When start oscillation (tSTA) + t_{HDL}

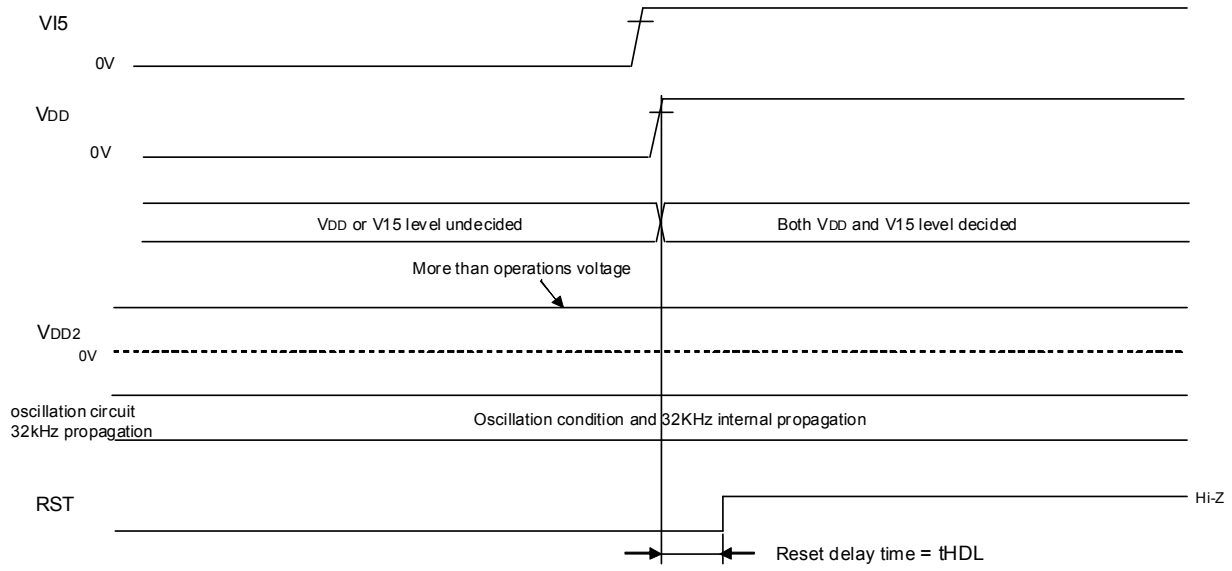
Reset delay time when work oscillation (32kHz internal propagation condition) is the following value.

- t_{HDL}

1) Reset delay time when start oscillation (V_{DD} from 0V or when input V_{DD2})



2) Reset delay time when oscillating (32kHz internal propagation condition)



[14] Internal Reset Function

14.1 Reset signal in EEPROM control circuit

Reset signal of EEPROM control circuit is formed with the following contents.

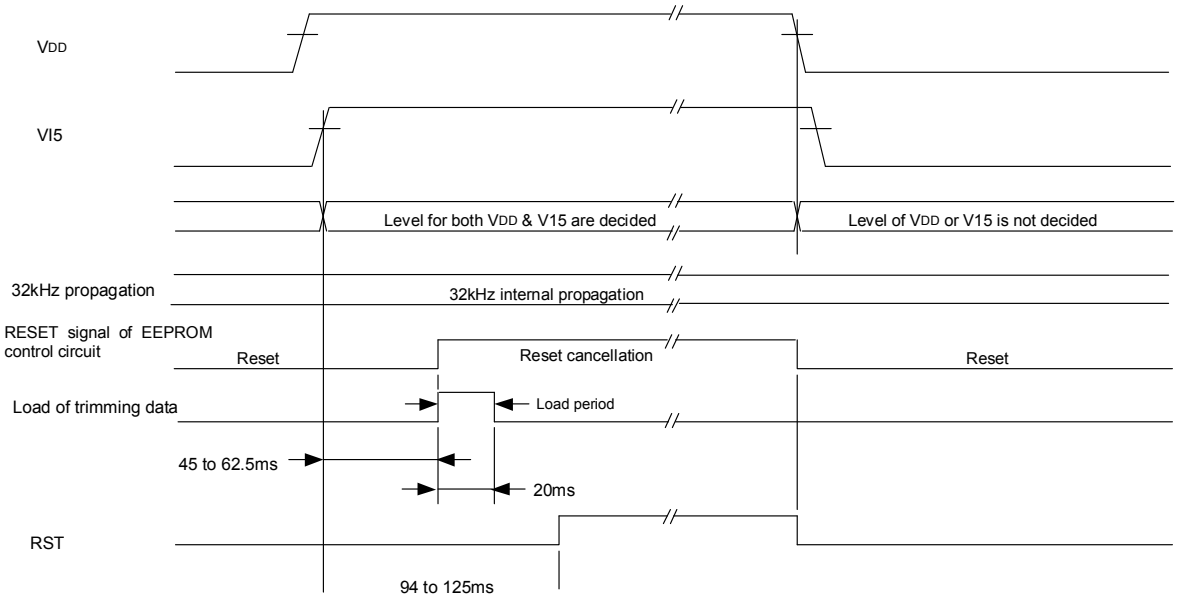
In case of one of the followings, give a reset to EEPROM control circuit .

1) When V_{DD} power(3.3V system) level is not decided.
2) When level of VI5 is not decided.
3) When 32kHz signal from oscillation circuit is not propagated to inner circuit of IC.
4) When FRST input (forced reset input) is High.

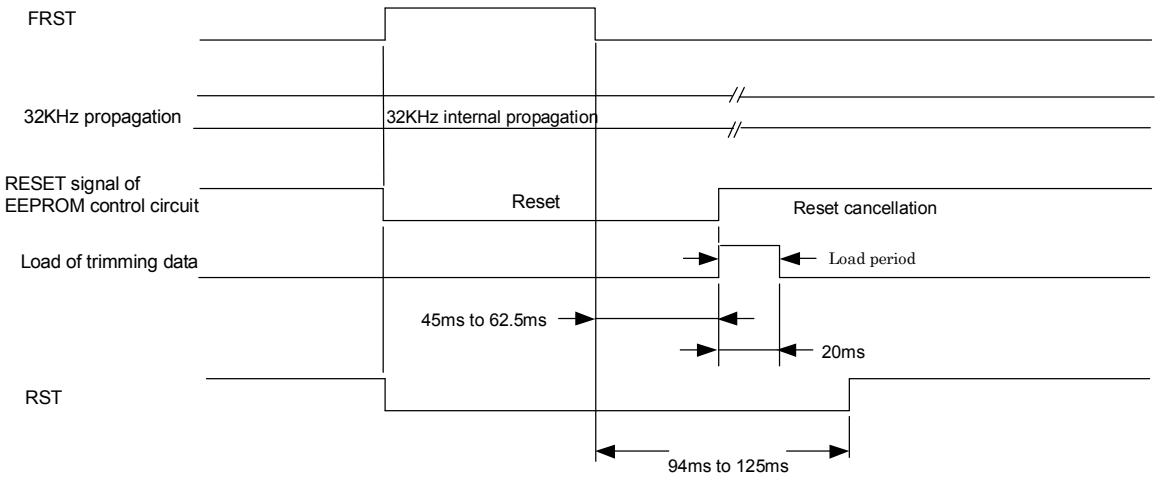
Reset of EEPROM control circuit is cancelled for the following two cases.

1) If meet all of the following 4 conditions, cancel reset of EEPROM control circuit part.
   - V_{DD} power (3.3V system)level is decided.
   - VI5 level is decided.
   - 32kHz signal from oscillation circuit is propagated to inner circuit of IC.
   - FRST input (forced reset input) is Low.
2) Reset cancellation by FRST input is in accordance with the following conditions.
   - 32kHz signal from oscillation circuit is propagated to inner circuit of IC.
   - When FRST input (forced reset input) is changed from High to Low. (V_{DD}=2.7V to 3.6V)

1) Reset cancellation timing and related signal when FRST input is Low and 32kHz signal is propagated to inner circuit of IC, and both V_{DD} and VI5 are detected level decision are shown below.



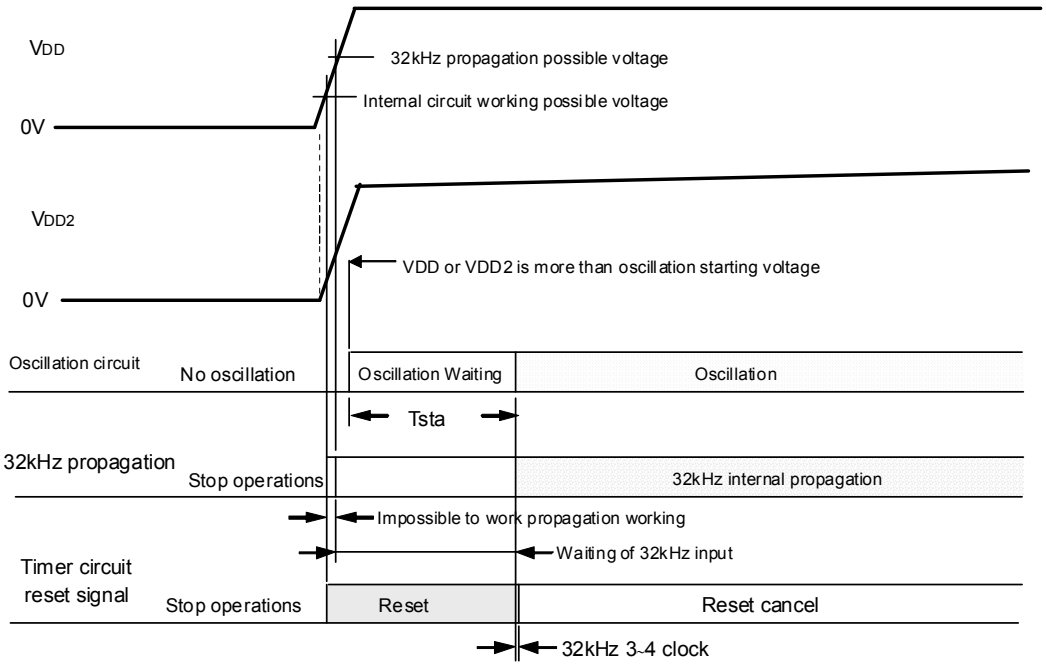
2) Reset cancellation timing and related signal when 32kHz signal is propagated to internal circuit of IC and when FRST input (forced reset input) is changed from High to Low (V_{DD}=2.7V to 3.6V) are shown below.



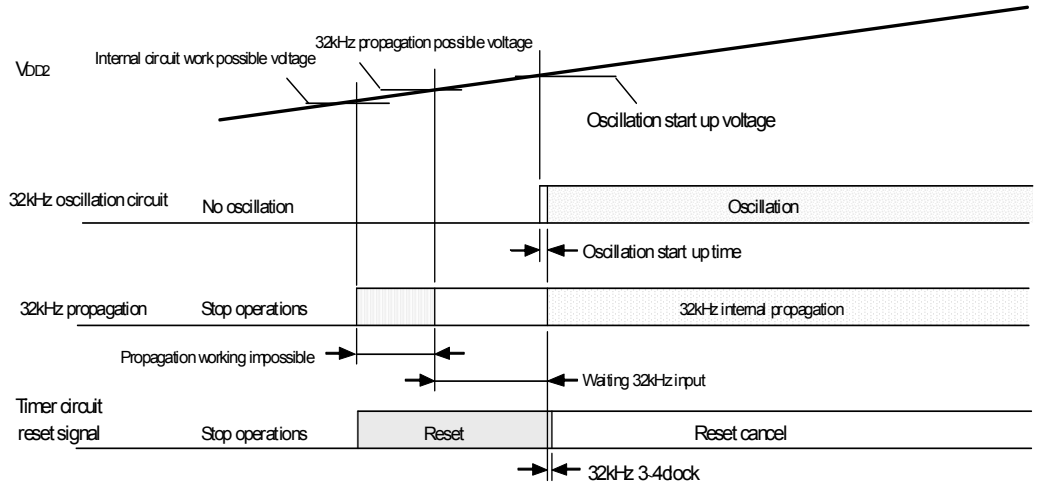
14.2 Reset signal of timer circuit

Reset signal of timer circuit except EEPROM control circuit is formed with the following content.
Reset signal of timer circuit is formed by detecting 32kHz clock from 32kHz oscillation circuit.
If impossible to detect 32kHz clock, gives reset. Addresses 0h to 3h are cleared by reset signal.
If 32kHz clock is detected, cancel reset.
Reset signal is formed with the following timing chart for each case when input V_{DD} and V_{DD2} from V_{DD2}=0V, V_{DD}=0V, when increase and drop voltage of power.

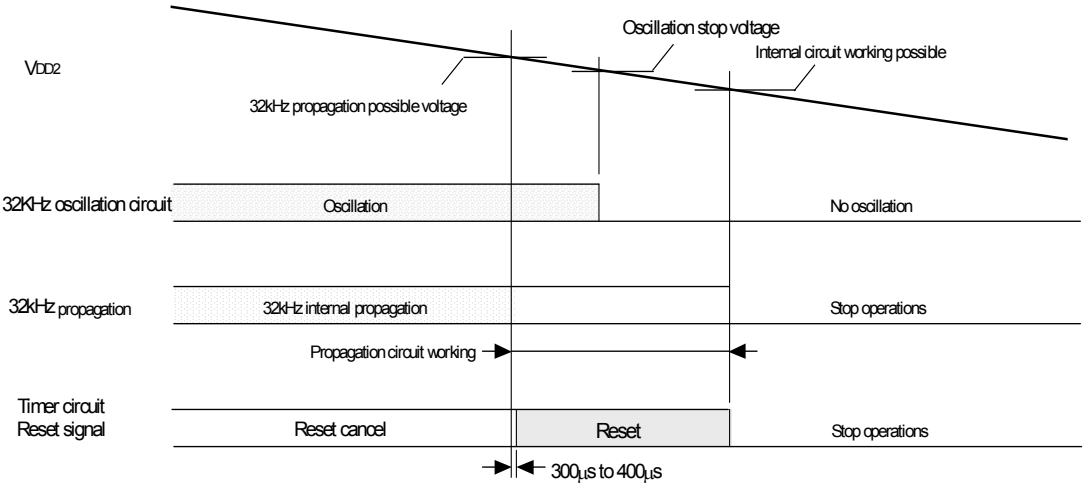
1) When input V_{DD}, V_{DD2} from V_{DD2}=0V, V_{DD}=0V.



2) When voltage of V_{DD2} power increases (V_{DD}=0V)



3) When falls voltage of V_{DD2} power (V_{DD}=0V)



[15] Voltage Regulator control function

32kHz oscillation circuit (OSC) and 32kHz clock detecting circuit (STPF Detect) is driven by regulation voltage (Vreg) power (Vcore) formed in internal IC. This voltage regulator for Vcore voltage formation (Vreg) is changed over to 3 mode such as boost mode, normal mode and backup mode when input (when start oscillation) V_{DD} or V_{DD2} power and by input voltage (VI5det) of VI5. Voltage regulator for Vcore voltage formation (Vreg) is worked by higher power either V_{DD} or V_{DD2}.

With boost mode, output high voltage to get quick oscillation start up time (t_{STA}).

Output low voltage by working sampling of Duty1/8 for saving power consumption.

Boost mode : 1.56V output, always operation
Normal mode : 1.02V output, always operation
Backup mode : 1.02V output, sampling operation

When input V_{DD} or V_{DD2} power (when start oscillation), output 1.8V. (V_{DD2}= over 1.8V)

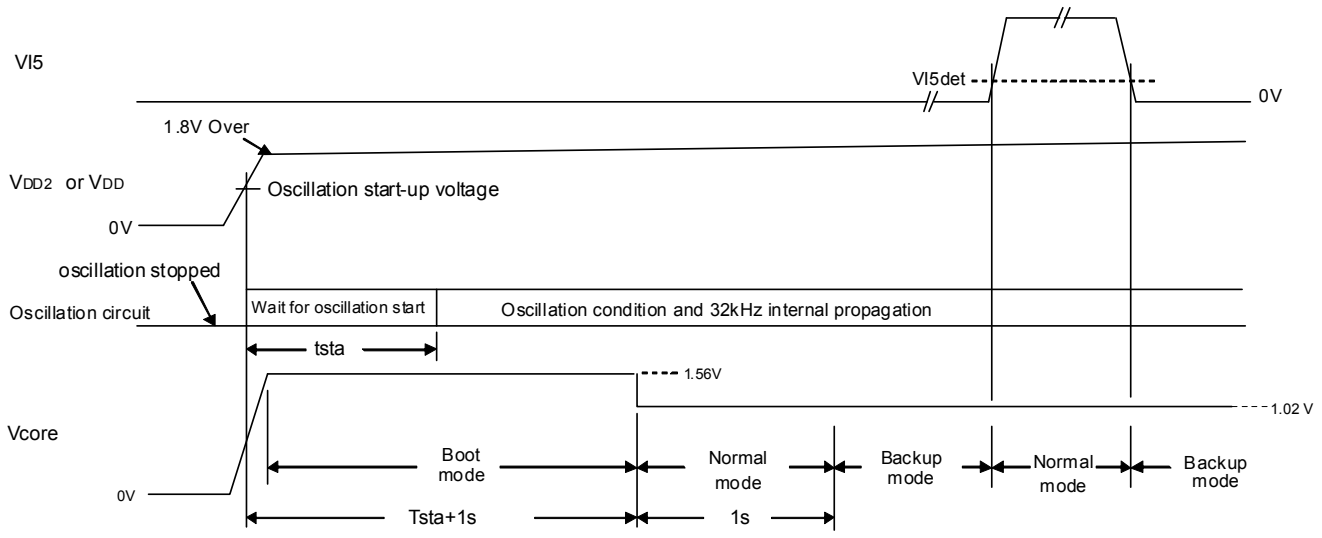
After [Oscillation start time (t_{STA})+1 second] from V_{DD} or V_{DD2} power input, output voltage is changed over to normal mode with 1.02V. After that, in case VI5 input voltage is less than VI5det, move to backup mode after 1 second and output voltage is changed over to 1.02V.

With backup mode, becomes to Duty1/8 sampling work.

When backup mode, VI5 input voltage becomes to over VI5det, change to normal mode.

In normal mode, if input voltage of VI5 becomes to less than VI5det, change over to backup mode.

∗ With backup mode, it works with ultra low power consumption. Be sure to refrain from sudden change of V_{DD} and V_{DD2} power.



Notes) Voltage value is guiding value only (Typ. value).

[16] Serial data transfer format

This transfers 4-line type (or 3-line type) serial data. Serial data is transferred using MSB First in the following order: mode, address, data.
Set the mode using the upper 4 bits (mode field), and the data length for each field (address data) that follows will be determined.

16.1 Mode field

Setting the mode using the upper 4 bits.

Mode field		m3	m2	m1	m0
		Read/Write	Reserved	BANK Reg.	
Data bit	0	0:Write	0*	00: Reserved 01: Timer mode 10: Reserved 11: Nonvolatile Memory	
	1	1:Read	0*		

∗m2 bit is able to Read/Write even if write ”1”, but please use with ”0”.
∗m0 bit is able to Read/Write even if write “0“ , but please use with ”1”.

16.2 Address field/Data field

Timer mode (m1 bit =0,m0 bit=1)

Mode field	m3	m2	m1	m0				
Address field	a3	a2	a1	a0				
Data field	d7	d6	d5	d4	d3	d2	d1	d0

Nonvolatile Memory (m1 bit=1,m0 bit=1)

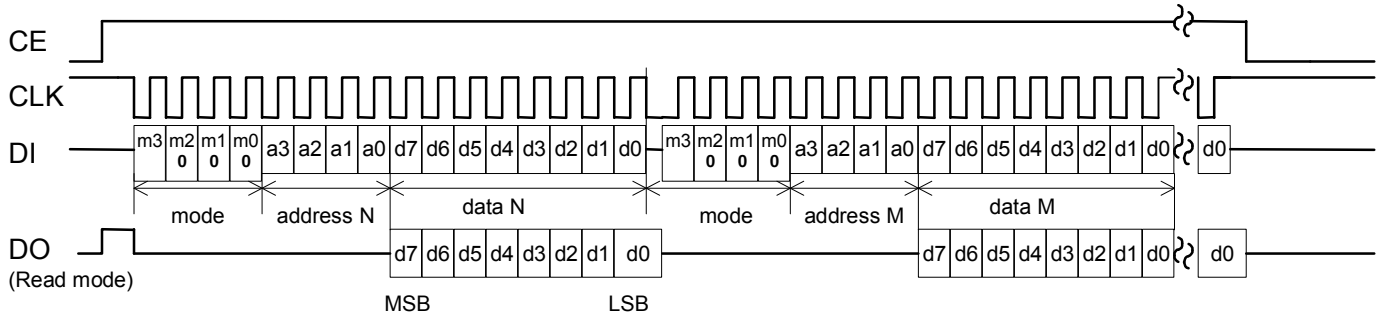
Mode field	m3	m2	m1	m0				
Address field	seg3	seg2	seg1	seg0				
	a7	a6	a5	a4	a3	a2	a1	a0
Data field	dF	dE	dD	dC	dB	dA	d9	d8
	d7	d6	d5	d4	d3	d2	d1	d0

∗Segment bit(seg3 to 0) is able to Read/Write even if write “1” , but be sure to use with “0” because of for expanded memory

16.3 Transfer mode

16.3.1 Cycle mode (Timer mode)

This module only provides Timer mode as a Cycle mode. Since it allows data reading and writing to be continued, this mode is useful for time data reading and flag overwriting (read and write).

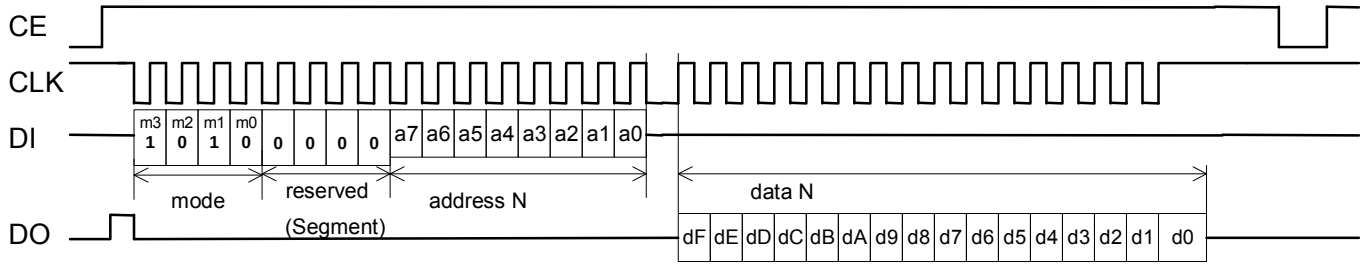


* During data transfer, Cannot switch to Nonvolatile Memory mode

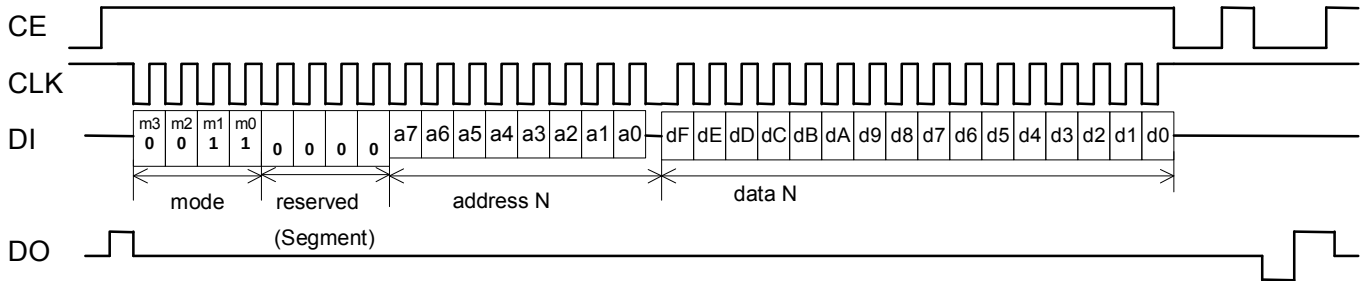
16.3.2 Nonvolatile Memory mode

Data can be transferred after the address is set.

- Read mode



- Write mode



[17] Access to Nonvolatile Memory (EEPROM)

It is possible to access to Nonvolatile Memory(EEPROM) if meet the following conditions.

1) V_{DD}=2.7V to 3.6V
2) VI5=VI5det over
3) When oscillation circuit is working and 32kHz clock is propagated to internal circuit.
4) When RSToutput is Hi-z(Reset cancellation).

[α+ t_{HDL}] later after deciding both V_{DD} and VI5.

When start oscillation : $\alpha=t_{STA}$(when start ascillation), when work oscillaition : α=0.

There are timing to load trimming data to adjust reference voltage to prescribed voltage range with 3 voltage detecting function of V_{DD}, VI5 and VEX. It is impossible to access to Nonvolatie Memory with timing of load trimming data, therefore please surely access after cancellation of external Reset (RST output is Hi-z) by RST output.

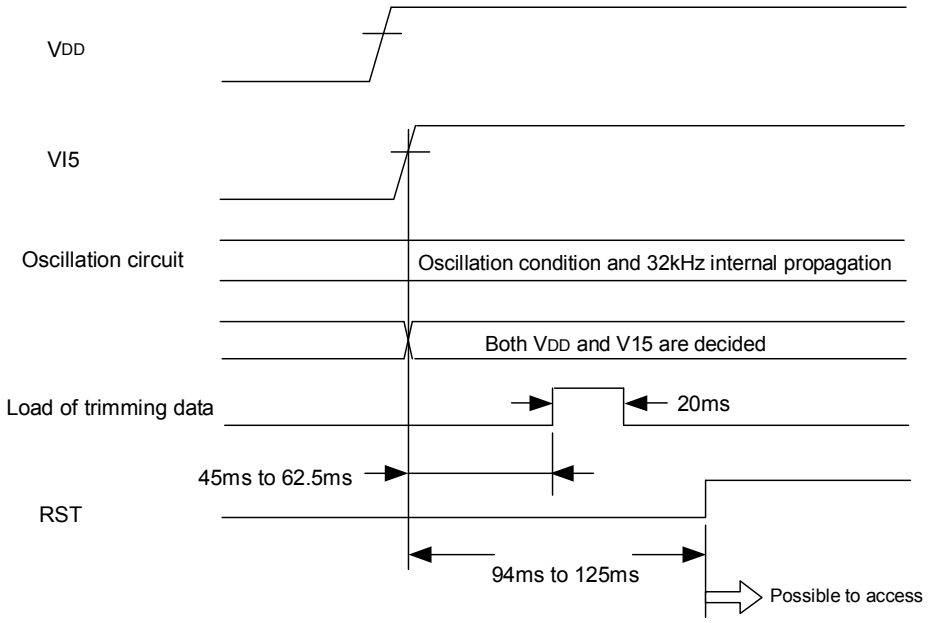
Timing to load trimming data from Nonvolatile Memory are the following 2 cases when oscillation circuit works and 32kHzclock is propagated to internal circuit.

1) When both voltage V_{DD} and VI5 are decided.
2) When FRST input (forced reset inout) is changed over from High to Low.

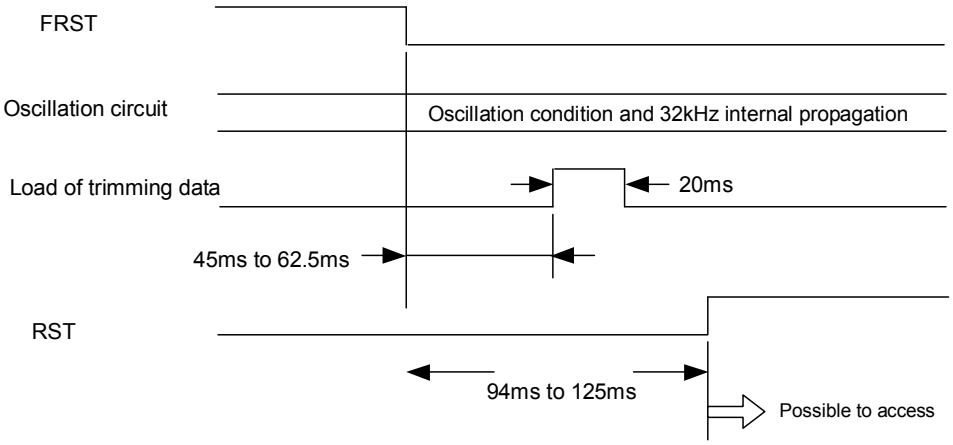
Time of loading is 20ms..

Timing to load trimming data and timing chart of RST output relation are shown below.

1) When both voltage level V_{DD} and VI5 are decided.



2) When both voltage V_{DD} and VI5 are decided.



* Load explanation of trimming data.

Trimming data works for adjusting referenece voltage with 3 voltage detecting function of V_{DD},VI5 and VEX to prescribed voltage range. Address housing trimming data write setting data with FEh and FFh when deliver factory.
Prohibited to write in this address.

[18] Register Functions Description

18.1 Registers

18.1.1 Nonvolatile Memory table (when using Nonvolatile Memory mode)

Segmemt	Address	Data																Comments
		dF	dE	dD	dC	dB	dA	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	
0	00	User Memory																4 kbit(254×16 bit)
	..																	
	7F																	
	80																	
	..																	
	FD																	
	FE	Reserved Memory																Factory default setting*
	FF	Reserved Memory																Don't write to this area.

* Do not write over memory reserved for the factory default setting.

18.1.2 Timer register

Addr	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
0	SEC	0	S40	S20	S10	S8	S4	S2	S1	R/W	BCD write
1	MIN	0	M40	M20	M10	M8	M4	M2	M1	R/W	BCD write
2	LTMR0	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0	R/W	BIN write
3	LTMR1	LT15	LT14	LT13	LT12	LT11	LT10	LT9	LT8	R/W	BIN write
4	LT Reg	OVF	LSEL1	LSEL0	-	LOF3	LOF2	LOF1	LOF0	R/W	
5	TEST Reg	TEST*2	-*4	-	-	-	-	-	-	R/W	
6	Flag Reg*3	STPF	0	-	-	0	EXF	-	-	R/W	
7	Control	-	0	-	-	0	-	VLIE*5	-	R/W	

∗1 Write “0” to the bit of “0” mark.
∗2 The TEST is utilized in Epson test. You should clear the TEST to "0" by all means.
When TEST is set to "1", the IC does functions abnormality.
∗3 As for STPF, only "0" clear is possible.
∗4 As for the bit of "-", write is impossible, and readout value is indefinite.
∗5 Clear the VLIE to "0" by all means. (There is not effect for the other function and a current even if write “1”.)
∗6 After initial power-on occurred, clear to "0" each bit of LOF0, LOF1, LOF2, LOF3, and VLIE.
∗7 When circuit (STPF Detect) detecting a crystal oscillation of 32kHz detects the stop of the clock of 32kHz, it is reset to address 0h-03h, and it is cleared to “0”.

18.2 VEX low voltage alarm (EXF)

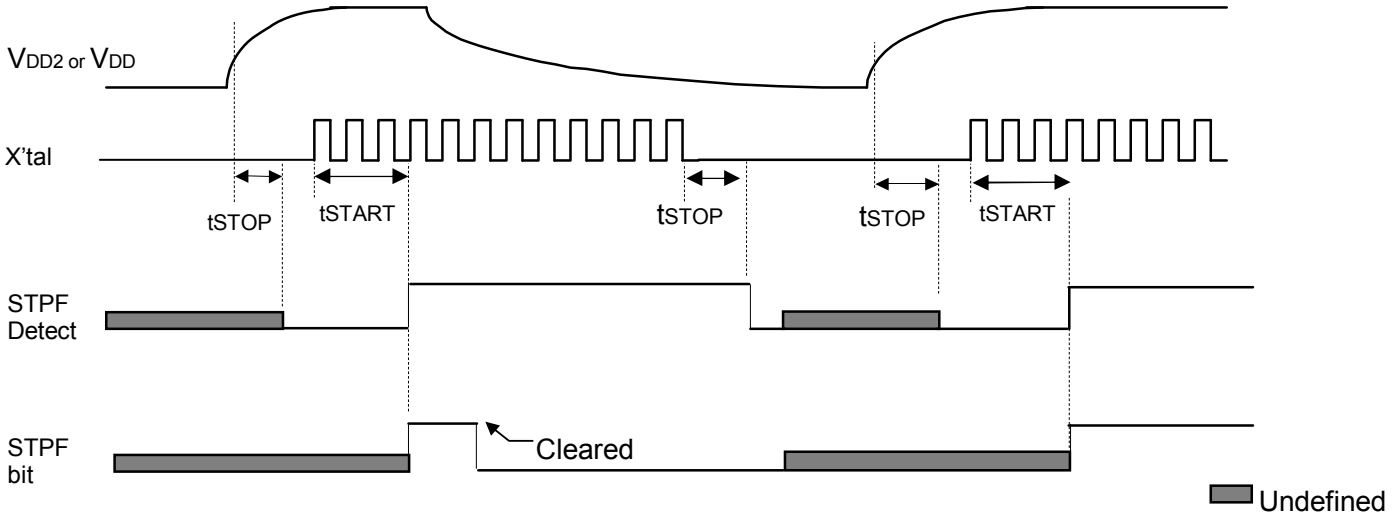
You can observe VEX voltage using an independent voltage detection circuit. This circuit allows constant high precision voltage monitoring, but remember that this consumes power.
The circuit's main applications are main battery (main power supply) voltage observation.
* When not in use, fix VEX to GND.

Reg.	bit data	Content	Comments
EXF		1: Detects voltages less than VEX.	Retained until a "0" is written.

18.3 Oscillation circuit voltage drop flag (STPF)

This function detects drops in voltage for the crystal oscillator. Previously, when a voltage drop occurred, STPF (Stop Flag) became "1". When STPF is "1", you must make initial settings because all registers are undefined except for nonvolatile memory.

Item	Symbol	condition	Min.	Typ.	Max.	Unit
Oscillation start detection time	tSTART	The period from a 32KHz clock input start			300	μs
Oscillation stop detection time	tSTOP	The period when the 32KHz clock stops			5000	μs



18.4 Control registers

18.4.1 TEST

This bit is reserved for testing work by Seiko Epson. Be sure to set it to 0.
A TEST bit is 1 , but the Read/Write access to a TEST register is possible.
There is the case that BUSY signal doesn't leave but when "TEST" is set to "1".
On this account, ignore the BUSY-signal at access to clear the TEST.
Example
Ignore BUSY & TEST readout → TEST=1=yes → Ignore BUSY & TEST clear to 0 →
→ TEST=0 confirmation readout.

18.4.2 VLIE

This circuit block is not equipped with RTC-9825B SA, therefore there is not increase of the current regardless of the state of the VLIE bit.

18.5 Flag registers

This register is a flag register. As each event occurs, the flag register is set to 1, and can be cleared by setting it to "0". To retain the state of the corresponding register, set it to "1" (mask).

18.5.1 STPF

This flag is a bit that records when the oscillation stopped. For details, refer to the Oscillation circuit voltage drop flog (STPF)

18.5.2 EXF

Becomes "1" when a VEX voltage drop occurs.

[19] Timer logic

This is a long timer for counting-up a clock that was set using LSEL.
Since the data for initial operation is undetermined, you must make initial settings.
Caution: Long timer is counted up synchronized with counting up of seconds and minutes register.
For this reason, error with max. one cycle time of selected source clock is occurred.
For example, in case of selecting source clock with 1 hour, there are two possibilities like 1 count up soon and 1 count up max. 59 minutes and 59 seconds later. If correct timer setting is needed, please synchronize second and minute register.

19.1 Timer register

Addr	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W	Comments
0	SEC	0	S40	S20	S10	S8	S4	S2	S1	R/W	BCD write
1	MIN	0	M40	M20	M10	M8	M4	M2	M1	R/W	BCD write
2	LTMR0	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0	R/W	BIN write
3	LTMR1	LT15	LT14	LT13	LT12	LT11	LT10	LT9	LT8	R/W	BIN write
4	LT Reg	OVF	LSEL1	LSEL0	-	LOF3	LOF2	LOF1	LOF0	R/W	
5	TEST Reg	TEST*2	-*4	-	-	-	-	-	-	R/W	
6	Flag Reg*3	STPF	0	-	-	0	EXF	-	-	R/W	
7	Control	-	0	-	-	0	-	VLIE*5	-	R/W	

∗1 Write “0” to the bit of “0” mark.
∗2 The TEST is utilized in Epson test. You should clear the TEST to "0" by all means.
When TEST is set to "1", the IC does functions abnormality.
∗3 As for STPF, only "0" clear is possible.
∗4 As for the bit of "-", write is impossible, and readout value is indefinite.
∗5 Clear the VLIE to "0" by all means. (There is not effect for the other function and a current even if write “1”.)
∗6 After initial power-on occurred, clear to "0" each bit of LOF0, LOF1, LOF2, LOF3, and VLIE.
∗7 When circuit (STPF Detect) detecting a crystal oscillation of 32kHz detects the stop of the clock of 32kHz, it is reset to address 0h-03h, and it is cleared to “0”.

19.2 Second and minute register (Address 0,1)

This is a 60-base BCD counter that counts from 0 to 59.
The counter is incremented when the digits increase from the lower register, and the digits in the upper register increase when the counter goes from 59 to 0. (When an incorrect value is set, such as 65, the increments are cleared to 0, and the digits in the upper register increase.)
When writing to second data, the counter for increments of less than a second is also cleared. Data is cleared immediately after DO data is “latched” to CLK.

	Reg.			Content	Comments
Source clock setting	LSEL1	LSEL0	Clock		
	0	0	1 s	1 second counter	
	0	1	1 min	1 minute counter	
	1	0	1 h	1 hour counter	
	1	1		Reserved	
Long Timer	LT15~0		By setting up of LSEL1,0	1~0xFF_FF(hex)	Long timer
Over flow	OVF		LT overflow bit		

[20] Operation condition of each function

	EEPROM access	Timer access	Timer function	External voltage detection circuit	External reset function	Oscillation
VDD	2.7 V to 3.6 V	2.7 V to 3.6 V	*2 2.7 V to 3.6 V	2.7 V to 3.6 V	2.7 V to 3.6 V	*2 2.7 V to 3.6 V
VI5	VI5det over	×	×	×	4.5 V to 5.5 V	×
VDD2	×	×	*3*4 1.4 V to 5.5 V	×	×	*3 1.8V to 5.5 V
32kHz	*1 Internal propagation	*1 Internal propagation	*1 Internal propagation	*1 Internal propagation	*1 Internal propagation	
RST output	Reset cancellation (Hi-z)	×	×	×		×

×: Don’t care
*1: Shows condition that works oscillation of 32kHz and propagates 32kHz clock into IC internal circuit.
*2: Or one of *3 keeps prescribed voltage.
*4: This is the voltage when VDD2 dropped after an oscillation start(1.8V ≤ VDD2).
When a circuit does not use the backup mode of the low current,

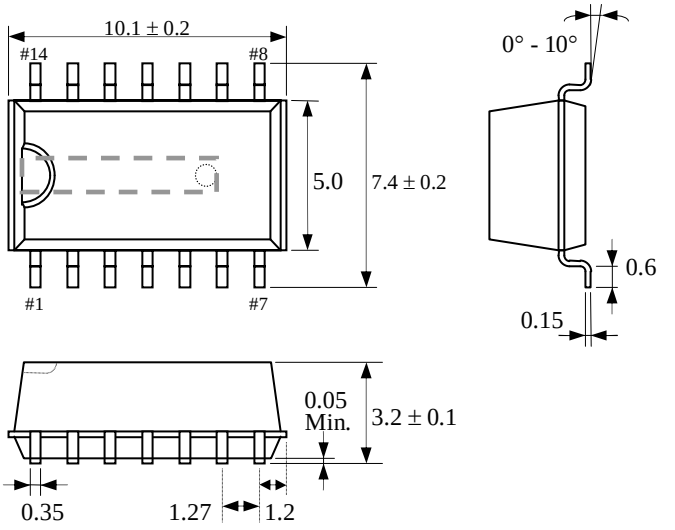
RTC works by impressing a power supply on VDD(2.7V~3.6V).

[21] External diagram

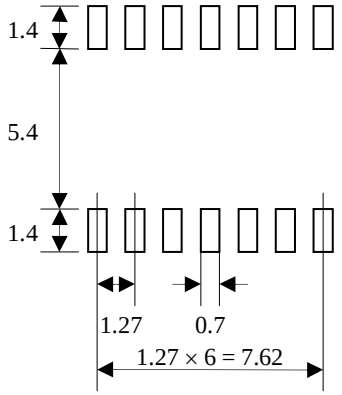
[SA] External diagram

RTC – 9825B SA (SOP – 14 pin)

• External dimensions



• Recommended soldering pattern

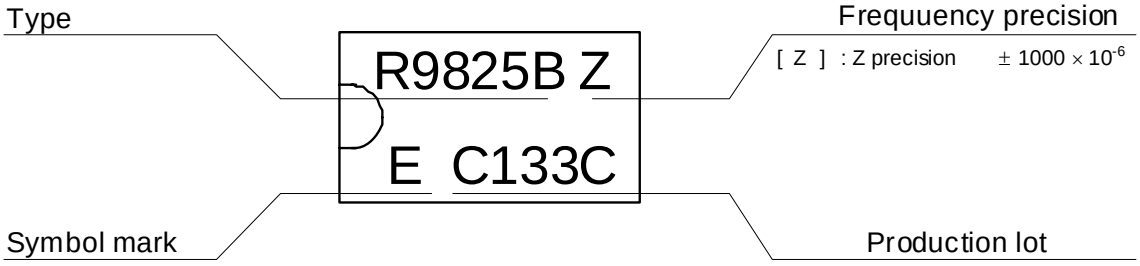


Unit : mm

∗ The cylinder of the crystal oscillator can be seen in this area (front), but it has no affect on the performance of the device.

Marking layout

RTC – 9825B SA (SOP – 14 pin)



C 13 3C

(1) (2) (3)

(1) One column of bottom of the Christian era
(Terminal lead-free)

(2) Production week

(3) Our control No.

Epoxy resin
(Halogen-free)
End Colum : C

∗ The correspondence list of the marking

One column of bottom of the Christian era	1	2	3	4	5	6	7	8	9	0
Marking (Terminal lead-free)	A	B	C	D	E	F	G	H	J	K

* The above illustration gives a general indication of markings. Actual character font, size, and position may differ.

[22] Environmental and mechanical characteristics

(The company evaluation condition We evaluate it by the following examination item and examination condition.)

No.	Item	Value *1		Test Conditions
		$\Delta f / f$ [1×10^{-6}] *2	Electrical characteristics	
1	High temperature storage	*3 ± 50	*4	+125 °C × 1 000 h
2	Low temperature storage	*3 ± 10		-55 °C × 1 000 h
3	High temperature bias	*3 ± 20		+85 °C × 5.5 V × 1 000 h
4	Low temperature bias	*3 ± 10		-40 °C × 5.5 V × 1 000 h
5	Temperature humidity bias	*3 ± 20		+85 °C × 85 %RH × 5.5 V × 1 000 h
6	Temperature cycle	*3 ± 10		-55 °C ⇔ +125 °C 30 min at each temp. 100 cycles
7	Resistance to soldering heat	± 5		For convention reflow soldering furnace (2 times)
8	Drop	± 5		Free drop from 750 mm height on a hard wooden board for 3 times (Board is thickness more than 30 mm)
9	Vibration	± 5		10 Hz to 55 Hz amplitude 0.75 mm 55 Hz to 500 Hz acceleration 98 m/s^2 10 Hz → 500 Hz → 10 Hz 15min./cycle 6 h (2 hours , 3 directions)
10	Flexibility of termination	No defect for wire termination		Put weight of 2.5 N on top of the termination Bending following angle :+90 ° to -90 ° to 0
11	Solderability	Termination must be 95 % covered with fresh solder		Dip termination into solder bath at +235 °C ± 5 °C for 5 s (Using Rosin Flux)
12	Solvent resistance	The marking shall be legible		Ref. JIS C 0052 or IEC 60068-2-45

< Notes >

*1 Each test done independently.

*2 Measuring 2 h to 24 h later leaving in room temperature after each test.

*3 Pre conditionings

1. +125 °C × 24 h to +85 °C × 85 % × 48 h → reflow 2 times
2. Initial value shall be after 24 h at room temperature.

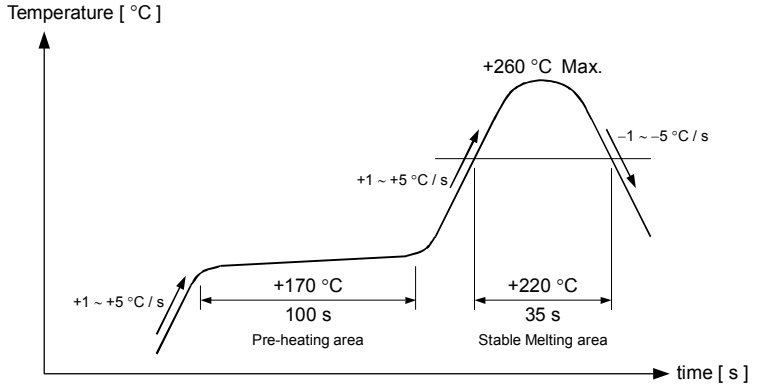
*4. After testing, Satisfies [5] Oscillation characteristics, and [6] ~[10] Electrical characteristics.
(Frequency precision and aging is excluded.)

♦ Air-reflow

Pre heating temperature: +170 °C Pre heating time: 100 s

Heating temperature : +220 °C Heating time : 35 s

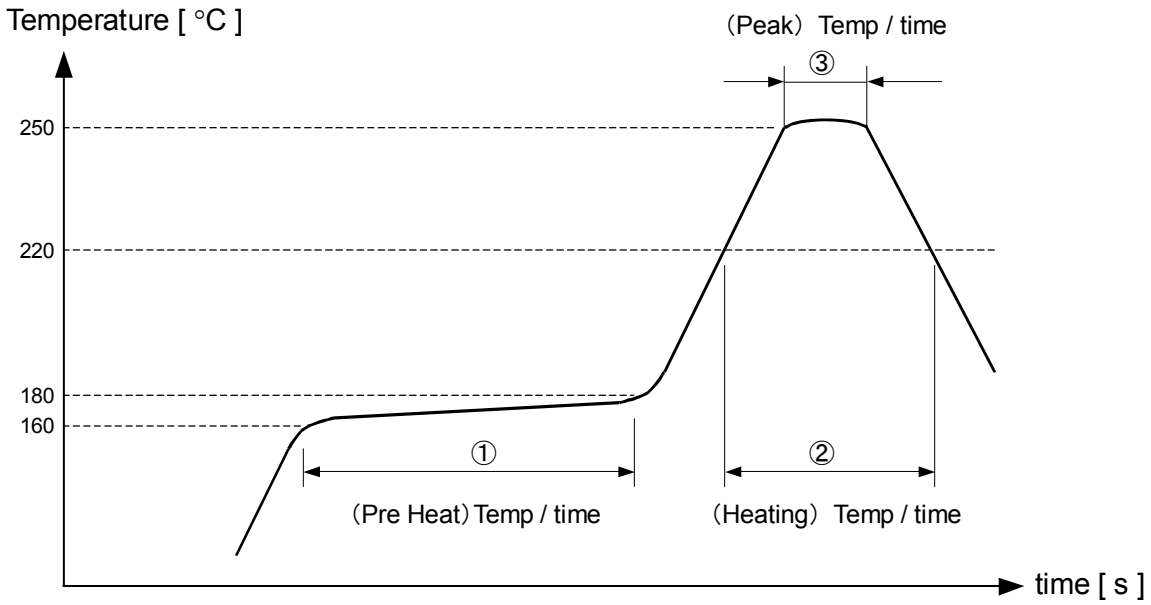
Peak temperature must not exceed +260 °C



[23] SEIKO EPSON reflow profile

(1) Air Reflow

① Pre Heating : +160 °C ~ +180 °C × 120 sec
② Heating : +220 °C × 60 sec
③ Peak : +250 °C × 10 sec



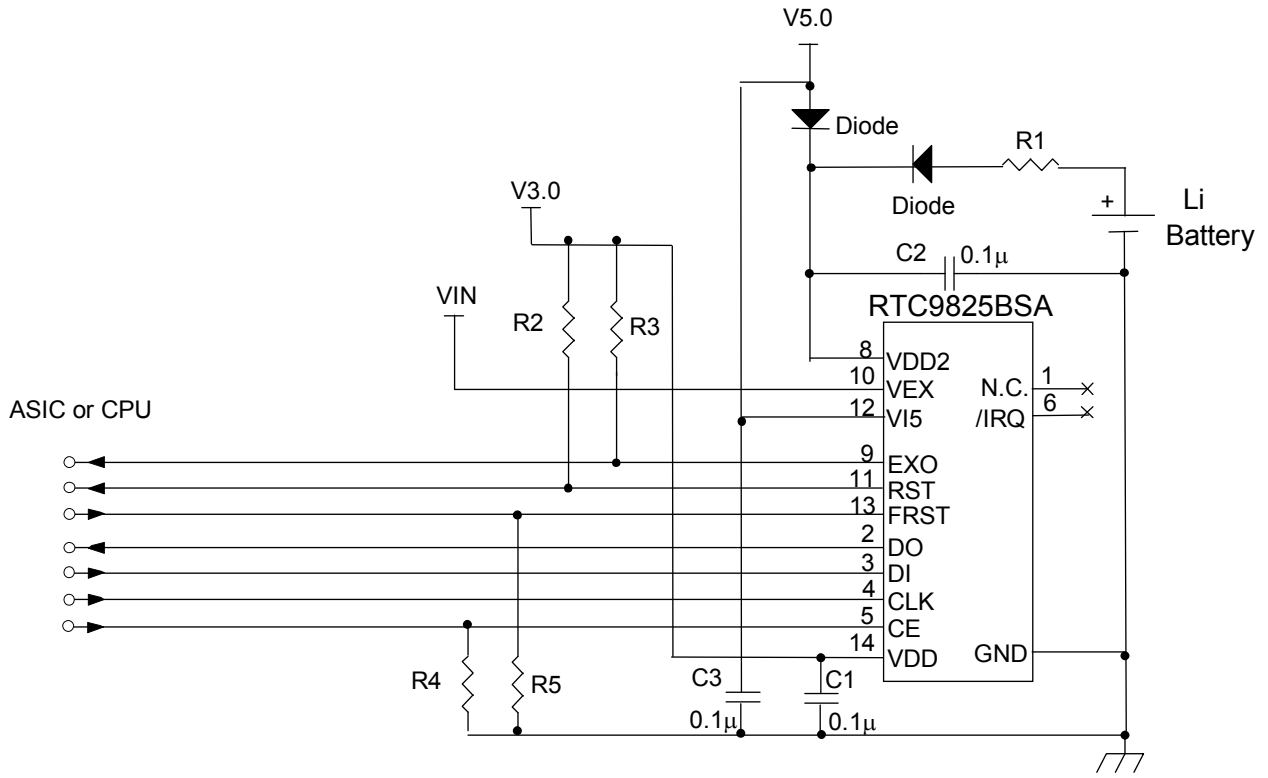
(2) Two (2) times reflow is allowed.

(3) Hand work soldering

+350 °C × within 3 sec (1 point) by soldering iron.

[24] External connection examples

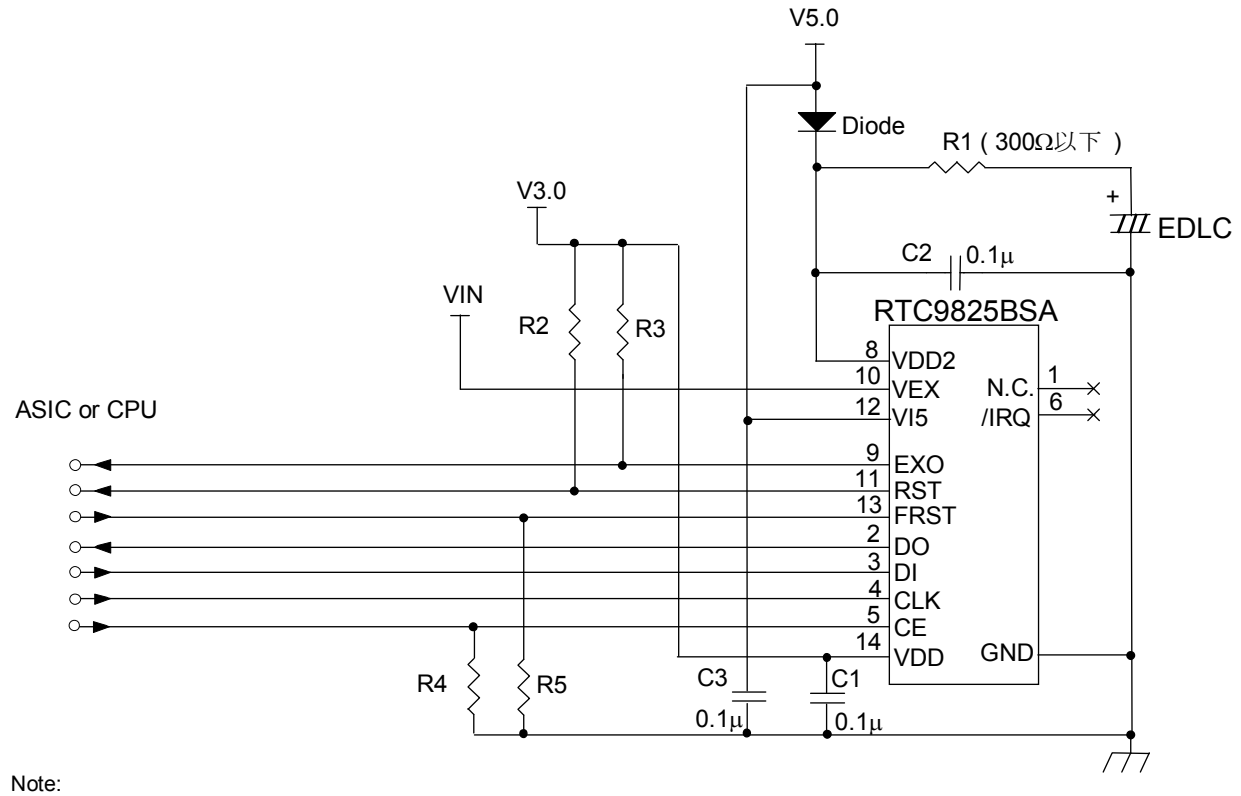
Example 1. Circuitry when using the primary battery



Note:

1. About the concrete value of a diode and the resistance, please choose it in consideration for UL standards.
2. Even if there is not a filter capacitor (C2), the circuit can guarantee a working, but recommends the connection of the filter capacitor for a safe design.

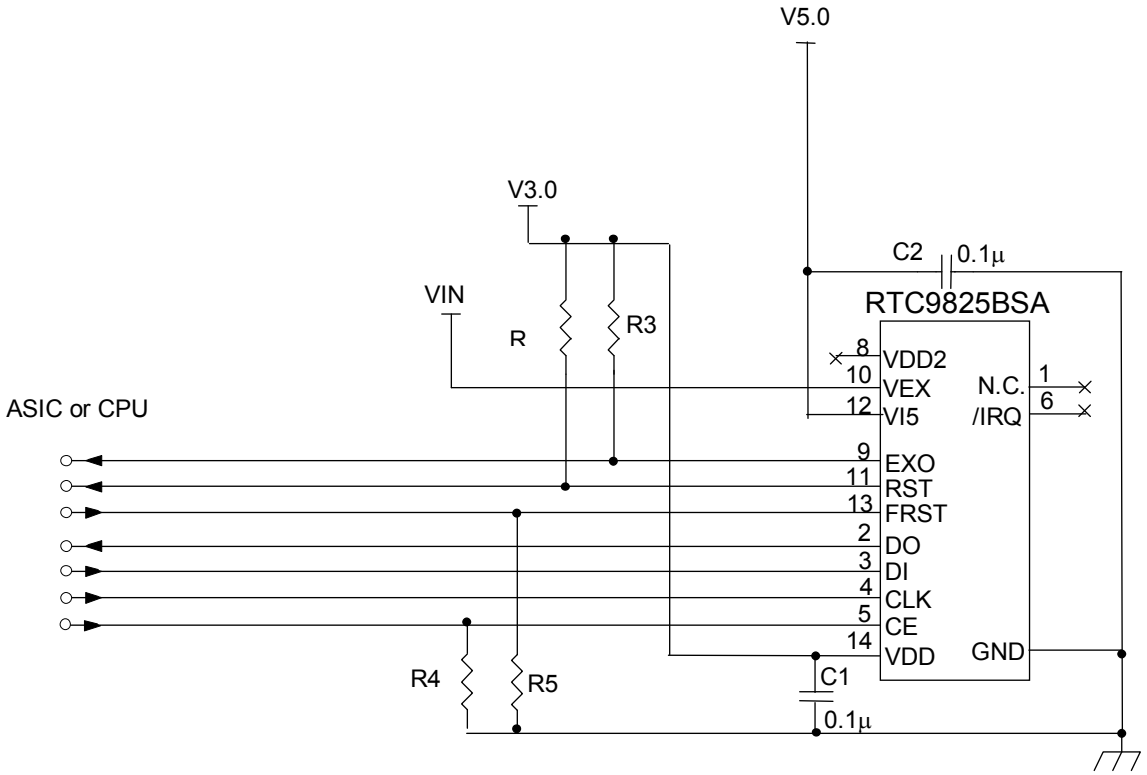
Example 2. Circuitry when using the Electric double-layer capacitor



Note:

Even if there is not a filter capacitor (C2), the circuit can guarantee a working, but recommends the connection of the filter capacitor for a safe design.

Example 3. Circuitry when not using the backup circuit.



[25] Notes on handling

1) Notes on handling

This module has a crystal oscillator built-in, and please do not give a module unreasonable shock / vibration.
This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity
While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise
If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1µF as close as possible to the power supply pins (between V_{DD} and GND, between V_{DD2} and GND). Also, avoid placing any device that generates high level of electronic noise near this module.
* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins
When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins
Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.
If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.
* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

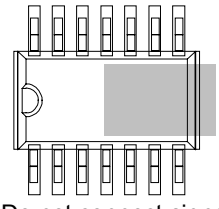
(2) Mounting equipment
While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning
Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

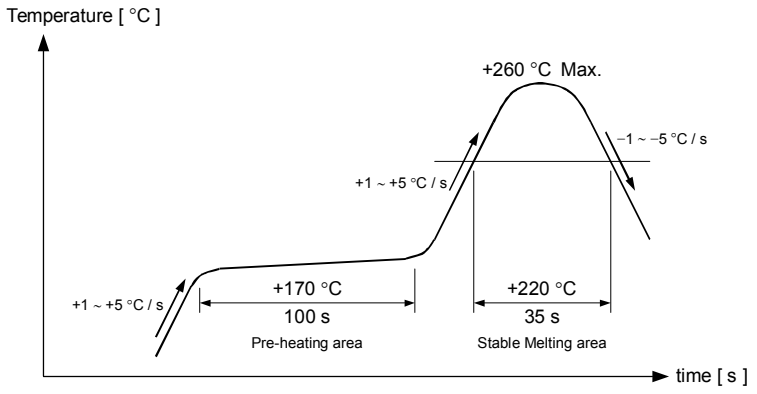
(5) Leakage between pins
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern



* Do not connect signal lines to the shaded area in the figure and, if possible, embed this area in a GND land.

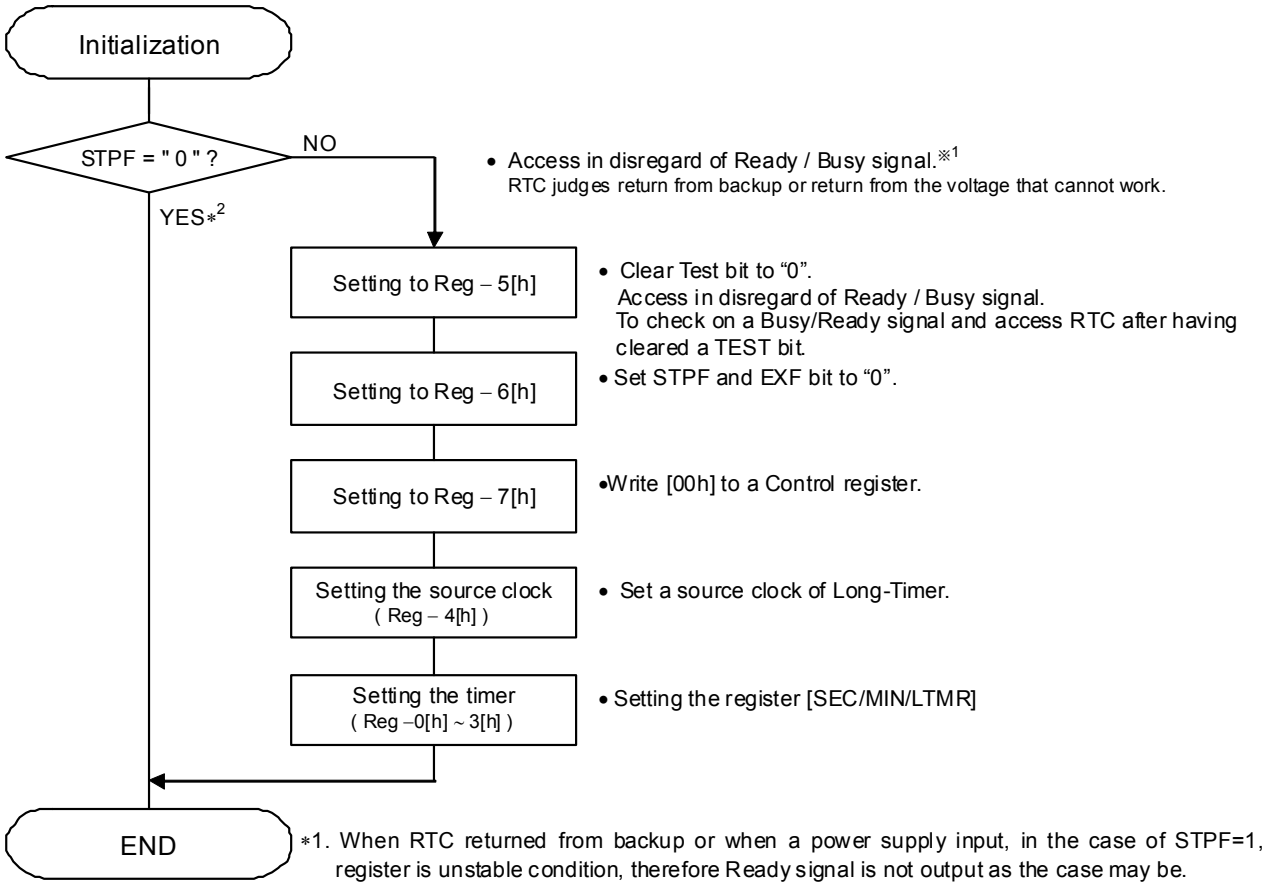
Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



[26] An example of the initialization

The following flow-chart is one instance. If you wish to take more efficient process, perform some processes at the same time or try to confirm and adjust some part where is no hindered from transposing of operation procedure.

Flow-chart



*1. When RTC returned from backup or when a power supply input, in the case of STPF=1, register is unstable condition, therefore Ready signal is not output as the case may be.

*2. Because it is the return from a backup state, in the case of STPF="0", RTC maintains setting.

TAPING SPECIFICATION

Ⅰ. Application

This standard will apply to SOP 14 pin package.

Spec：SA package

Ⅱ. Contents

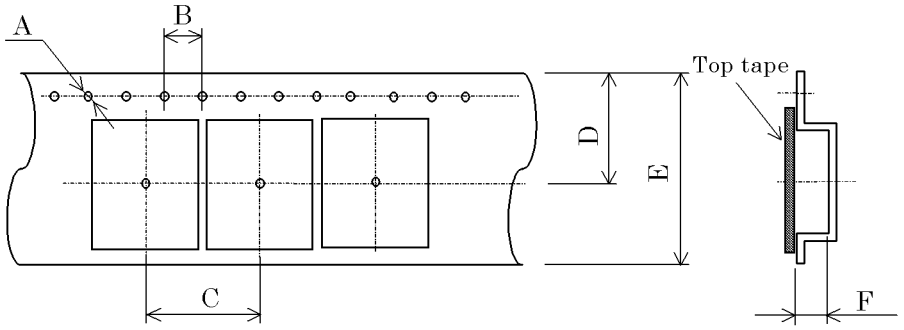
〔1〕 Taping specification

Subject to EIA-481& IEC 60286

(1) Tape dimensions TE-1612L

Material of the carrier tape : PS

Material of the top tape : PET

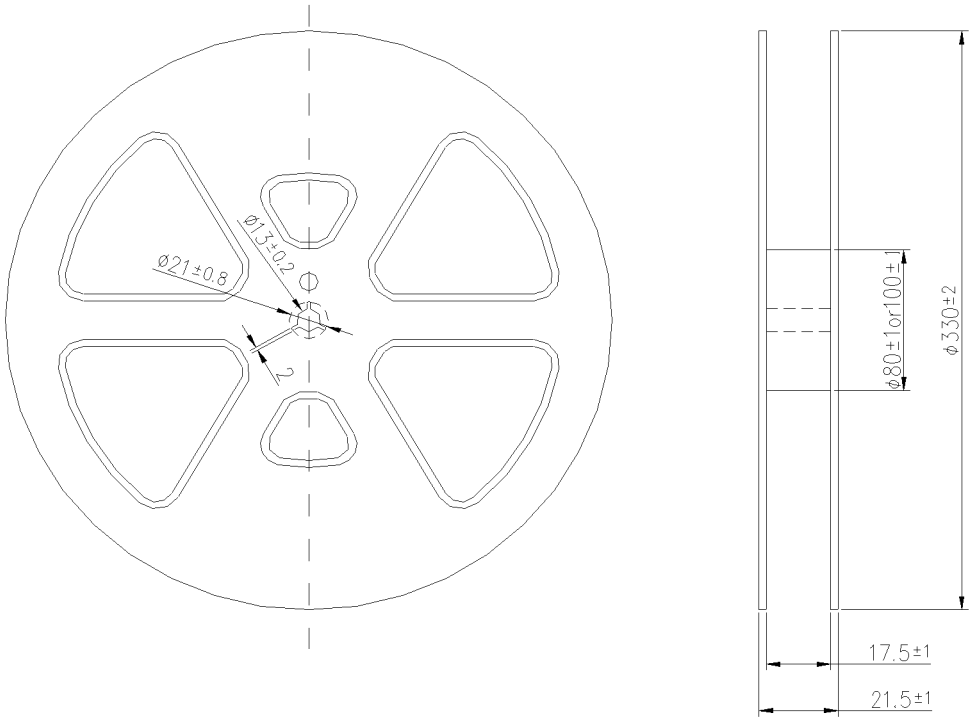


Symbol	A	B	C	D	E	F
Value	ϕ 1.5	4.0	12.0	9.25	16.0	3.65

Unit : mm

(2) Reel dimensions

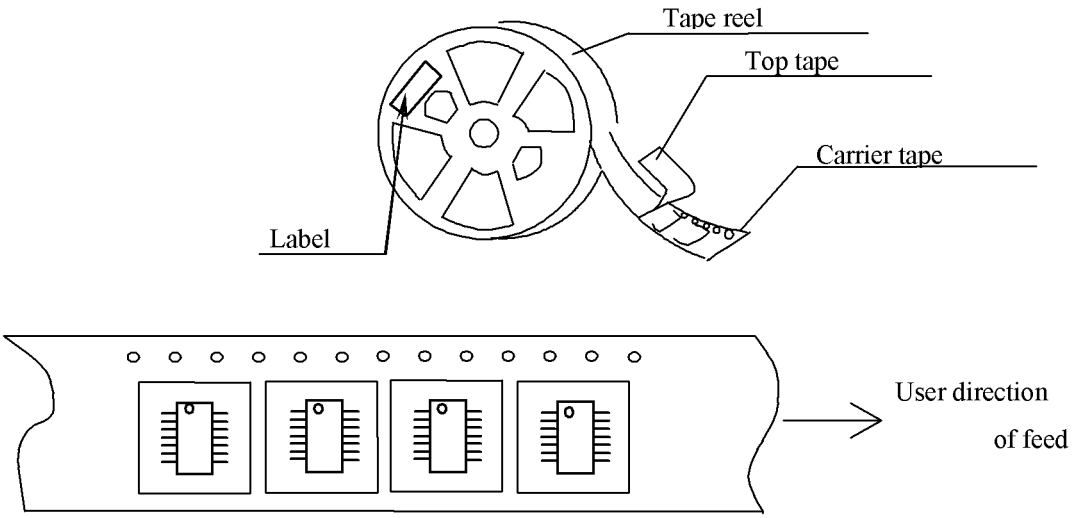
Material of the reel : Conductive polystyrene



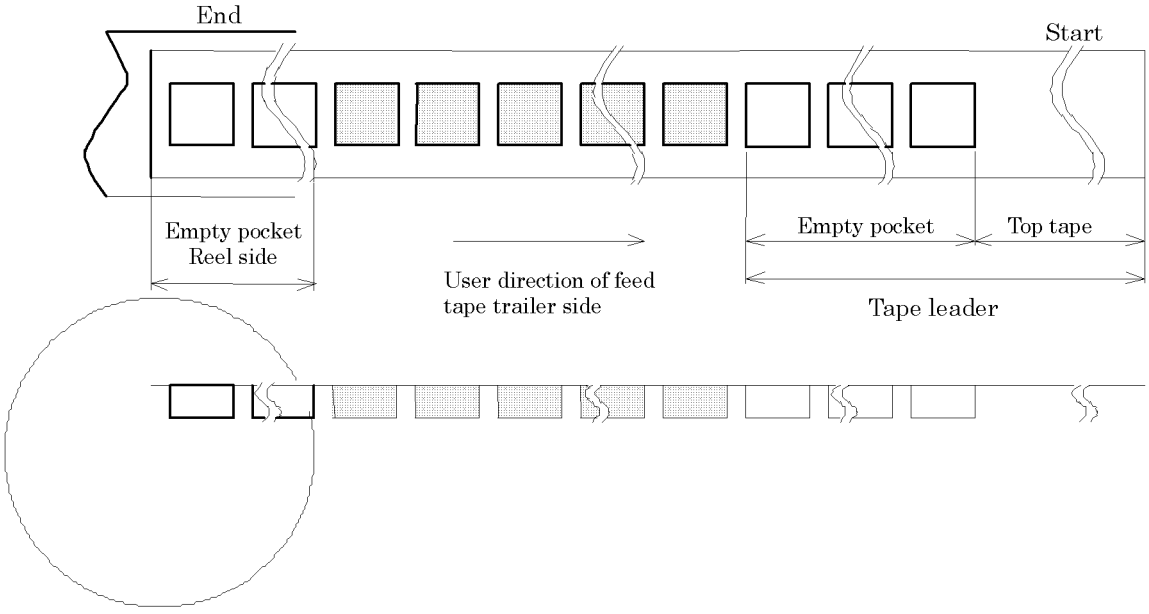
Form and Size of reel window shows are one of the example

(3) Packing ⚠

①Tape & reel



②Start & end point



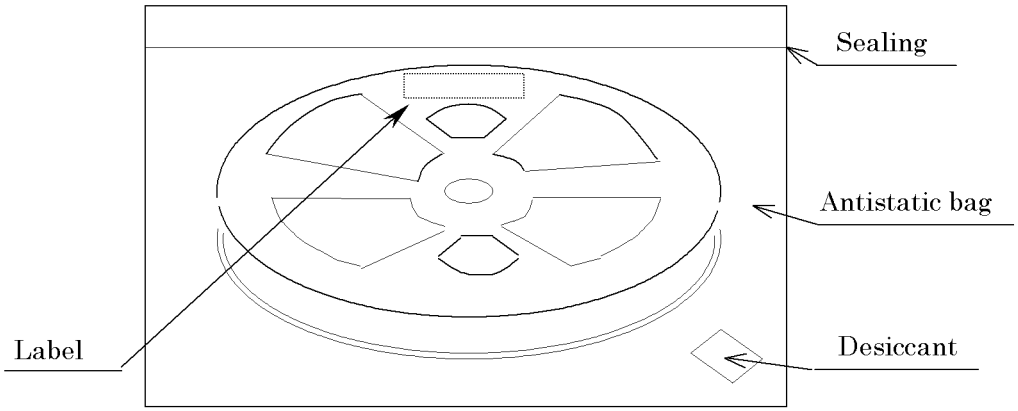
Item		Empty space	Note
Tape leader (Start side)	Top tape	Min. 1 000 mm	Feeding in the Top tape, the tip is fixed with tape.
	Carrier tape	Min. 120 mm	Winding method is a diagram of the above
Tape trailer (Reel side)	Top tape	Min. 0 mm	Tip is fixed to the reel.
	Carrier tape	Min. 120 mm	

〔2〕 Inner carton

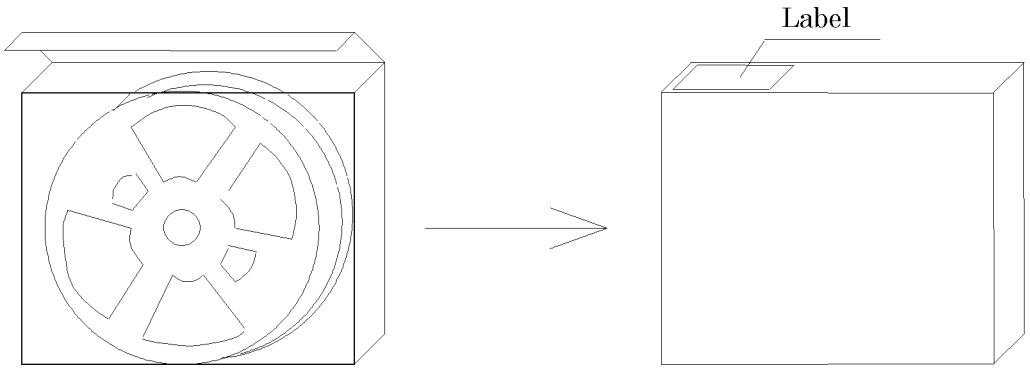
・After the reel bag, put a desiccant, to seal in the heat.

・Add to the inner box

a) Packing to antistatic bag



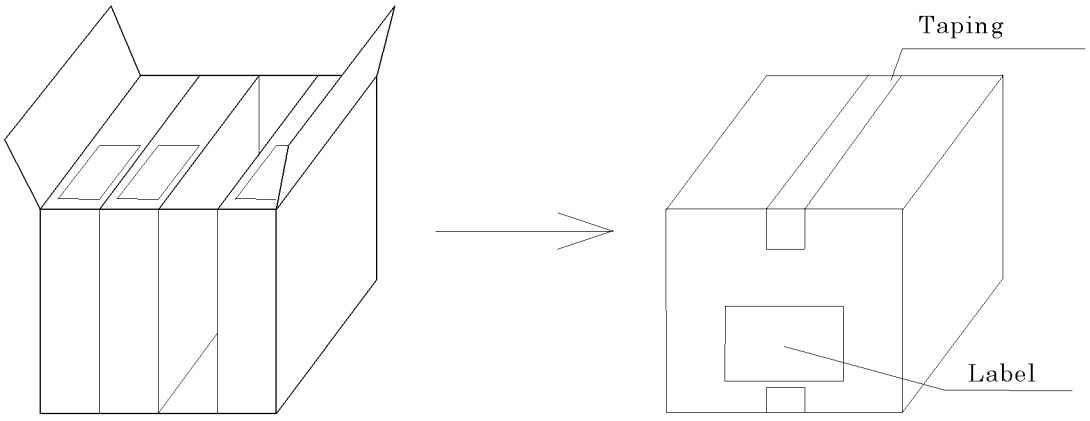
b) Packing to inner carton



〔3〕 Shipping carton

・Put in the inner carton to shipping carton.

・Gap is when you are, to put the cushion material.



〔4〕 Marking

(1) Reel marking

・Reel marking shall consist of :

1) Parts name
2) Quantity
3) Manufacturing date or symbol
4) Manufacturer's date or symbol
5) Others (if necessary)

(2) Inner carton marking

・Same as reel marking.

(3) Shipping carton marking

・Shipping carton marking shall consist of :

1) Parts name
2) Quantity

〔5〕 Quantity

・1 000 pcs./reel

〔6〕 Storage environment

(1) To storage the reel at 5 °C to 35 °C, 45 %RH to 85 %RH of humidity.
(2) To open the packing just before using.
After unpacking, please keep in moisture-proof container desiccant.
(3) Not to expose the sun.
(4) Not to storage with some erosive chemicals.
(5) Nothing is allowed to put on the reel or carton to prevent mechanical damage.

〔7〕 Handling

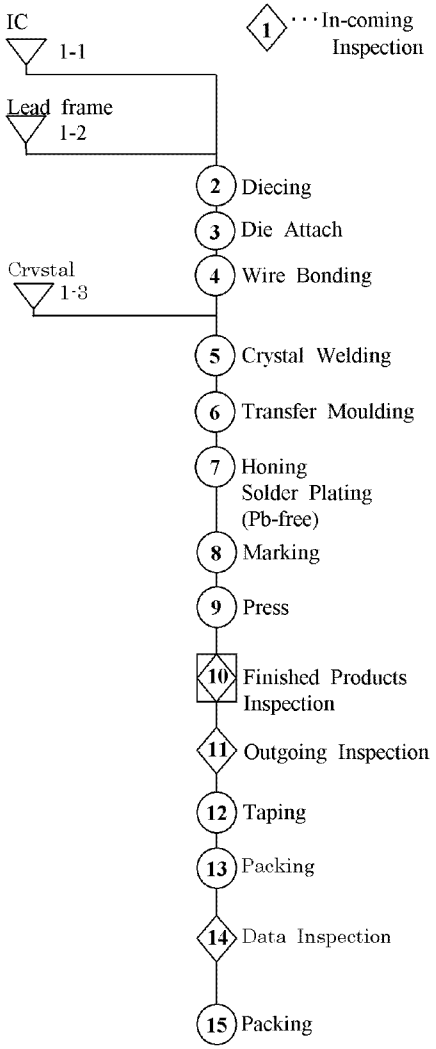
・To handle with care to prevent the damage of tape, reel and products.

- PROCESS QUALITY CONTROL -

RTC
Japan: KATOH Electric Co., Ltd. 6392 Kamiyoshida,Fujiyoshida-shi,Yamanashi,Japan

No. SOP14-00-Pb-ATE-1 SOP 14 pin

2007.4.19



No.	Section In charge	Standards & Specifications	Inspection & Control Item	Inspection Instruments	Inspection methods	Record
1	Inspection section	Purchasing specification Incoming Inspection standard	Appearance Dimension	Microscope	Sampling	Data Sheet
1-1	Subcontractor company	Incoming Inspection standard	Model,Quantity	Visual inspection	Sampling	Data sheet
1-2	Subcontractor company	Incoming Inspection standard	Model,Quantity, Appearance	Visual inspection	Sampling	Data sheet
2	Subcontractor company	The assembly delivery specification	Deionized water (resistivity) Appearance	Resistivity meter Microscope	Sampling	Data sheet
3	Subcontractor company	The assembly delivery specification	Appearance Die-share strength Dry-temperature,time	Microscope Thermometer,Timer	Sampling	Data sheet
4	Subcontractor company	The assembly delivery specification	Wire-pull strength Bonding strength Appearance Temperature,Force U.S.power	Pull-tester Ball-share tester Thermometer,Gauge Dial-gauge Microscope	Sampling	Data sheet
1-3	Subcontractor company	Incoming inspection standerd	Model,Quantity	Visual inspection	Sampling	Data sheet
5	Subcontractor company	The assembly delivery specification	Welding-power Pressure,Crystal position Appearance	Power-measure Gauge Microscope	Sampling	Data sheet
6	Subcontractor company	The assembly delivery specification	Mould Die-temperature Curing-Temperature,Time Appearance	Surface-thermometer Thermometer,Timer X-ray radio graphic equipment Visual Inspection	Sampling 100% Inspection	Data sheet
7	Subcontractor company	Outer appearance inspection standard	Plating thickness Appearance	Fluorescent X-ray Visual inspection	Sampling	Data sheet
8	Subcontractor company	Outer appearance inspection standard	Appearance	Image Processor	100% Inspection	Data sheet
9	Subcontractor company	Outer appearance inspection standard	Appearance Dimension	Image Processor	100% Inspection	Data sheet
10	Subcontractor company	Manufacturing Instruction sheet	Electrical characteristics Appearance	Measuring equipment	100% Inspection	Data sheet
11	Subcontractor company	Finished products Inspection standard	Electrical characteristics Outward from dimension Appearance	Measuring equipment Microscope	Sampling	Data sheet
12	Subcontractor company	The assembly delivery specification	Tape peeling force Appearance	Peeling force test machine Image Processor	Sampling 100% Inspection	Data sheet
13	Subcontractor company	Packing specification	———	———	———	———
14	Inspection section	Delivery specification outgoing Inspection standerd	Electrical characteristics Appearance	———	Every Lot	———
15	Production control section	Manufacturing Instruction sheet Daily shipping list	Customers Type Quantity	———	———	Delivery slip

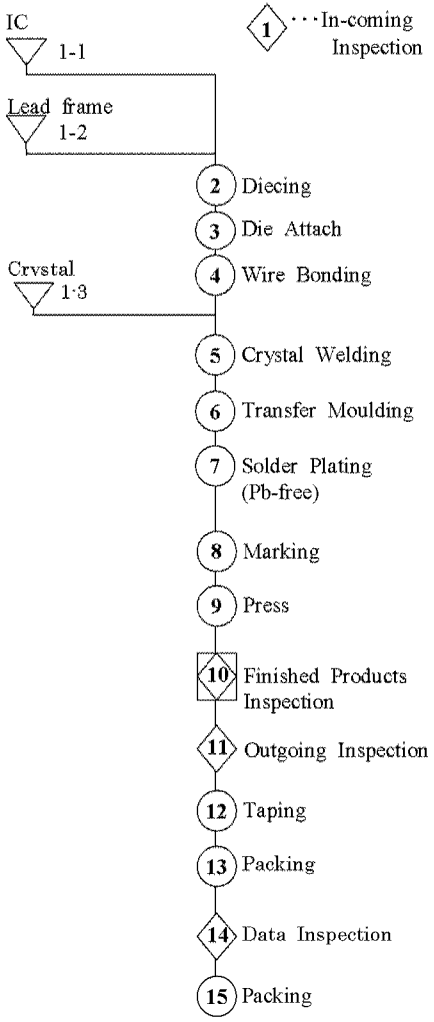
RTC

- PROCESS QUALITY CONTROL -

Japan: AOI ELECTRONICS CO/, LTD. 455-1 Takamatsu-shi,Kagawa,Japan

No. 4543SA - 00 - PbF - AAE – 2 **Real Time Clock Module SOP 14pin**

2003.12.17



No.	Section In charge	Standards & Specifications	Inspection & Control Item	Inspection Instruments	Inspection methods	Record
1	Inspection section	Purchasing specification Incoming Inspection standard	Appearance Dimension	Microscope	Sampling	Data Sheet
1-1	Subcontractor company	Incoming Inspection standard	Model,Quantity	Visual inspection	Sampling	Data sheet
1-2	Subcontractor company	Incoming Inspection standard	Model,Quantity, Appearance	Visual inspection	Sampling	Data sheet
2	Subcontractor company	The assembly delivery specification	Appearance	Visual inspection	Sampling	Data sheet
3	Subcontractor company	The assembly delivery specification	Appearance Die-share strength Dry-temperature,time	Visual inspection Gauge Thermometer,Timer	Sampling	Data sheet
4	Subcontractor company	The assembly delivery specification	Wire-pull strength Bonding strength Appearance Temperature,Force U.S.power	Pull-tester Ball-share tester Microscope Thermometer,Gauge Dial-gauge	Sampling	Data sheet
1-3	Subcontractor company	Incoming inspection standerd	Model,Quantity	Visual inspection	Sampling	Data sheet
5	Subcontractor company	The assembly delivery specification	Welding-power Pressure,Crystal position Appearance	Power-measure Gauge Microscope	Sampling	Data sheet
6	Subcontractor company	The assembly delivery specification	Shape of bonded wire Mould Die-temperature Curing-Temperature,Time Appearance	X-ray radio graphic equipment Surface-thermometer Thermometer,Timer Visual Inspection	Sampling 100% Inspection	Data sheet
7	Subcontractor company	Solder plating specification	Plating thickness Appearance	Fluorescent X-ray Visual inspection	Sampling 100% inspection	Data sheet
8	Subcontractor company	The assembly delivery specification	Appearance	Visual inspection	Sampling	Data sheet
9	Subcontractor company	The assembly delivery specification	Appearance Dimension	Visual inspection Microscope	Sampling	Data sheet
10	Subcontractor company	The assembly delivery specification	Electrical characteristics Appearance	Measuring equipment Visual inspection	100% Inspection	Data sheet
11	Subcontractor company	Finished products Inspection standard	Electrical characteristics Appearance	Measuring equipment Visual inspection	Sampling	Data sheet
12	Subcontractor company	The assembly delivery specification	Tape peeling force	Peeling force test machine	Sampling	Data sheet
13	Subcontractor company	The assembly delivery specification	———	———	———	———
14	Inspection section	Delivery specification outgoing Inspection standerd	Electrical characteristics Appearance	———	100% Inspection	———
15	Production control section	Manufacturing Instruction sheet Daily shipping list	Customers Type Quantity	———	———	Delivery slip

PROCESS QUALITY CONTROL

Crystal Unit
Japan:INA plant 8548 Nakaminowa,Minowa-machi,Kamiina-gun,Nagano,Japan

A-88-2-HIE-1

Manufacturing process chart	No.	Section In Charge	Standards	Inspection, Control Item	Inspection Methods	Instruments	Record
CRYSTAL BLOCK ① In-coming Inspection	1	Inspection Section	Purchasing Specification, Acceptance Inspection Standard	Appearance Dimension	Sampling Sampling	Visual Inspection Length Gauge	In-coming Inspection Data Sheet
①' In-coming Inspection	1'	Inspection Section	Purchasing Specification, Acceptance Inspection Standard	Dimension Appearance	Sampling Sampling	Comparator Microscope	In-coming Inspection Data Sheet
② Wafer Cutting	2	INA Plant	Manufacturing Instruction Sheet	Cut Angle Dimension	Sampling 100% Inspection	X-ray Radio Graphic Equipment,Comparator	Process Data Sheet
③ Wafer Polishing	3	INA Plant	Manufacturing Instruction Sheet	Appearance Wafer Thickness	100% Inspection Sampling	Visual Inspection Comparator	Process Data Sheet
④ Wafer Inspection	4	INA Plant	Manufacturing Instruction Sheet	Appearance	100% Inspection	Visual Inspection	Process Data Sheet
⑤ Profile Etching	5	INA Plant	Manufacturing Instruction Sheet	Etching Shape Dimension	Sampling Sampling	Microscope Comparator	Process Data Sheet
⑥ Electrode Processing (Sputtering)	6	INA Plant	Manufacturing Instruction Sheet	Film Thickness Film Strength Appearance	Sampling Sampling Sampling	Thickness Measuring Instrument, Tape Microscope	Process Data Sheet
⑦ SiO2 Coating	7	INA Plant	Manufacturing Instruction Sheet	Film Thickness Film Strength Appearance	Sampling Sampling Sampling	Thickness Measuring Instrument, Tape Microscope	Process Data Sheet
Plug ① In-Coming Inspection ⑧ Crystal Tuning Fork Inspection	8	INA Plant	Manufacturing Instruction Sheet	Frequency Appearance	100% Inspection 100% Inspection	Frequency Inspection Machine, Microscope	Process Data Sheet
Case ① In-Coming Inspection ⑨ Mounting	9	INA Plant	Manufacturing Instruction Sheet	Mount Strength Appearance	Sampling Sampling	Tension Gauge Microscope	Process Data Sheet
⑩ Frequency Adjustment	10	INA Plant	Manufacturing Instruction Sheet	Frequency	Sampling	Frequency Counter	Process Data Sheet
⑪ Annealing	11	INA Plant	Manufacturing Instruction Sheet	Temp・Time	Sampling	Thermometer, Timer	Process Data Sheet
⑫ Hermetic Sealing (Encapsulation)	12	INA Plant	Manufacturing Instruction Sheet	Dimension Appearance	Sampling Sampling	Comparator Microscope	Process Data Sheet
⑬ Products Inspection	13	INA Plant	Manufacturing Instruction Sheet	Electric Characteristics	100% Inspection	Characteristics Inspection Machine	Process Data Sheet
⑭ Counting and Packing To MC Line	14	INA Plant	Manufacturing Instruction Sheet Shipment List	Quantity Customer	----	----	Shipment List

Crystal Unit
Malaysia:EPMY Lot 1,Jalan Persiaran Industri, Taman Perindustrian
Sri Damansara, Sungai Buloh,52200 Kuala Lumpur

PROCESS QUALITY CONTROL

CODE:C-002SH

23/Jan/2001

Control No. A－88－2－HAEE-1

Manufacturing process chart	No.	Section In Charge	Standards	Inspection, Control Item	Inspection Methods	Instruments	Record
CRYSTAL BLOCK	1	Inspection Section	Purchasing Specification, Acceptance Inspection Standard	Appearance Dimension	Sampling Sampling	Visual Inspection Length Gauge	In-coming Inspection Data Sheet
▽ In-coming Inspection	1'	〃	〃	Dimension Appearance	Sampling 〃	Comparator Microscope	〃
② Wafer Cutting	2	2'nd Plant of Domestic in Japan	Manufacturing Instruction Sheet	Cut Angle Dimension	Sampling 100% Inspection	X-ray Radio Graphic Equipment,Comparator	Process Data Sheet
③ Wafer Polishing	3	〃	〃	Appearance Wafer Thickness	100% Inspection Sampling	Visual Inspection Comparator	〃
④ Wafer Inspection	4	〃	〃	Appearance	100% Inspection	Visual Inspection	〃
⑤ Profile Etching	5	〃	〃	Etching Shape Dimension	Sampling 〃	Microscope Comparator	〃
⑥ Electrode Processing (Sputtering)	6	〃	〃	Film Thickness Film Strength Appearance	Sampling 〃 〃	Thickness Measuring Instrument, Tape Microscope	〃
Plug ▽ ① In-Coming Inspection ⑦ Sio2 Coating	7	〃	〃	Film Thickness Film Strength Appearance	Sampling 〃 〃	Thickness Measuring Instrument, Tape Microscope	〃
⑧ Crystal Tuning Fork Inspection	8	Malaysia Plant	〃	Frequency Appearance	100% Inspection 〃	Frequency Inspection Machine, Microscope	〃
Case ▽ ① In-Coming Inspection ⑨ Mounting	9	〃	〃	Mount Strength Appearance	Sampling	Tension Gauge Microscope	〃
⑩ Frequency Adjustment	10	〃	〃	Frequency	Sampling	Frequency Counter	〃
⑪ Annealling	11	〃	〃	Temp・Time	Sampling	Thermometer, Timer	〃
⑫ Hermetic Sealing (Encapsulation)	12	〃	〃	Dimension Appearance	Sampling	Comparator Microscope	〃
⑬ Products Inspection	13	〃	〃	Electric Characteristics	100% Inspection	Characteristics Inspection Machine	〃
⑭ Counting and Packing	14	〃	〃 Shipment List	Quantity Customer	―――	―――	Shipment List
▽ To MC Line							

2'nd Plant AEC or MIYAZAKI

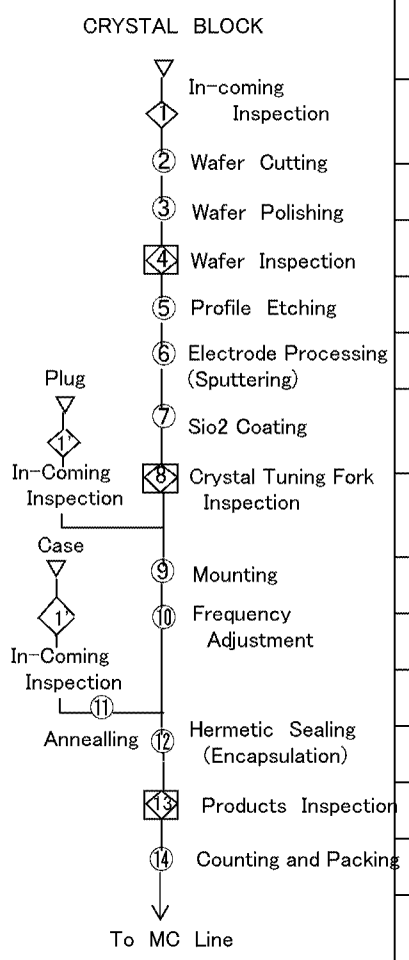
PROCESS QUALITY CONTROL

Crystal Unit
China: ETSZ No.144, Hua Shan Road, Suzhou New District, Suzhou, Jiangsu China

CODE:C-002SH

19/Feb/2001

Control No. A－88－2－HSE－1



No.	Section In Charge	Standards	Inspection, Control Item	Inspection Methods	Instruments	Record
1	Inspection Section	Purchasing Specification, Acceptance Inspection Standard	Appearance Dimension	Sampling Sampling	Visual Inspection Length Gauge	In-coming Inspection Data Sheet
1'	Inspection Section	Purchasing Specification, Acceptance Inspection Standard	Dimension Appearance	Sampling Sampling	Comparator Microscope	In-coming Inspection Data Sheet
2	2'nd Plant of Domestic in Japan	Manufacturing Instruction Sheet	Cut Angle Dimension	Sampling 100% Inspection	X-ray Radio Graphic Equipment,Comparator	Process Data Sheet
3	2'nd Plant of Domestic in Japan	Manufacturing Instruction Sheet	Appearance Wafer Thickness	100% Inspection Sampling	Visual Inspection Comparator	Process Data Sheet
4	2'nd Plant of Domestic in Japan	Manufacturing Instruction Sheet	Appearance	100% Inspection	Visual Inspection	Process Data Sheet
5	2'nd Plant of Domestic in Japan	Manufacturing Instruction Sheet	Etching Shape Dimension	Sampling Sampling	Microscope Comparator	Process Data Sheet
6	2'nd Plant of Domestic in Japan	Manufacturing Instruction Sheet	Film Thickness Film Strength Appearance	Sampling Sampling Sampling	Thickness Measuring Instrument, Tape Microscope	Process Data Sheet
7	China Plant	Manufacturing Instruction Sheet	Film Thickness Film Strength Appearance	Sampling Sampling Sampling	Thickness Measuring Instrument, Tape Microscope	Process Data Sheet
8	China Plant	Manufacturing Instruction Sheet	Frequency Appearance	100% Inspection 100% Inspection	Frequency Inspection Machine, Microscope	Process Data Sheet
9	China Plant	Manufacturing Instruction Sheet	Mount Strength Appearance	Sampling	Tension Gauge Microscope	Process Data Sheet
10	China Plant	Manufacturing Instruction Sheet	Frequency	Sampling	Frequency Counter	Process Data Sheet
11	China Plant	Manufacturing Instruction Sheet	Temp・Time	Sampling	Thermometer. Timer	Process Data Sheet
12	China Plant	Manufacturing Instruction Sheet	Dimension Appearance	Sampling	Comparator Microscope	Process Data Sheet
13	China Plant	Manufacturing Instruction Sheet	Electric Characteristics	100% Inspection	Characteristics Inspection Machine	Process Data Sheet
14	China Plant	Manufacturing Instruction Sheet Shipment List	Quantity Customer	――	――	Shipment List

2'nd Plant AEC or MIYAZAKI