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Application Manual

Programmable Voltage Controlled Oscillator

VG7050ECN

OUT-13-0626

SEIKO EPSON CORPORATION

(Rev.1.1)

NOTICE

(Rev.1.1)

Table of Contents

1. Overview

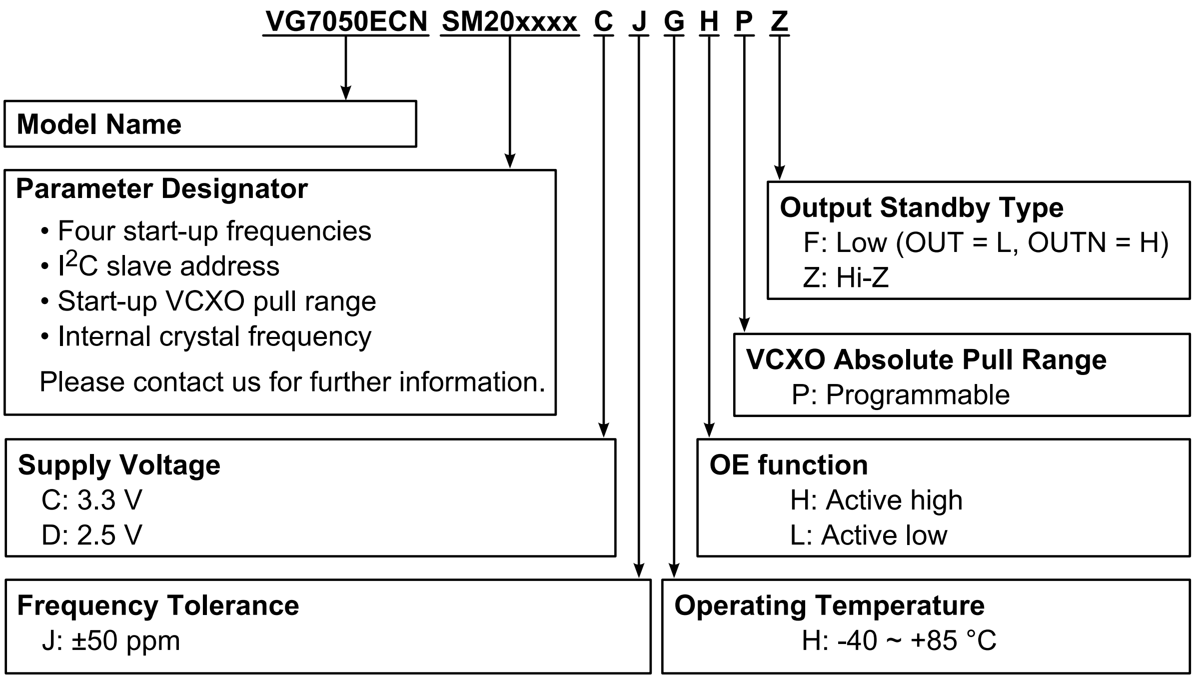
Programmable Voltage Controlled Oscillator: VG7050ECN is a low jitter programmable VCXO at any frequency. VG7050ECN consists of VCXO, PLL and LVPECL output buffer. Its output frequency is programmable from 50 MHz to 800 MHz with almost 2 ppb resolution.

VCXO supplies stable reference clock to PLL with fundamental tone crystal. Kv of VCXO can be programmed via I^2C interface.

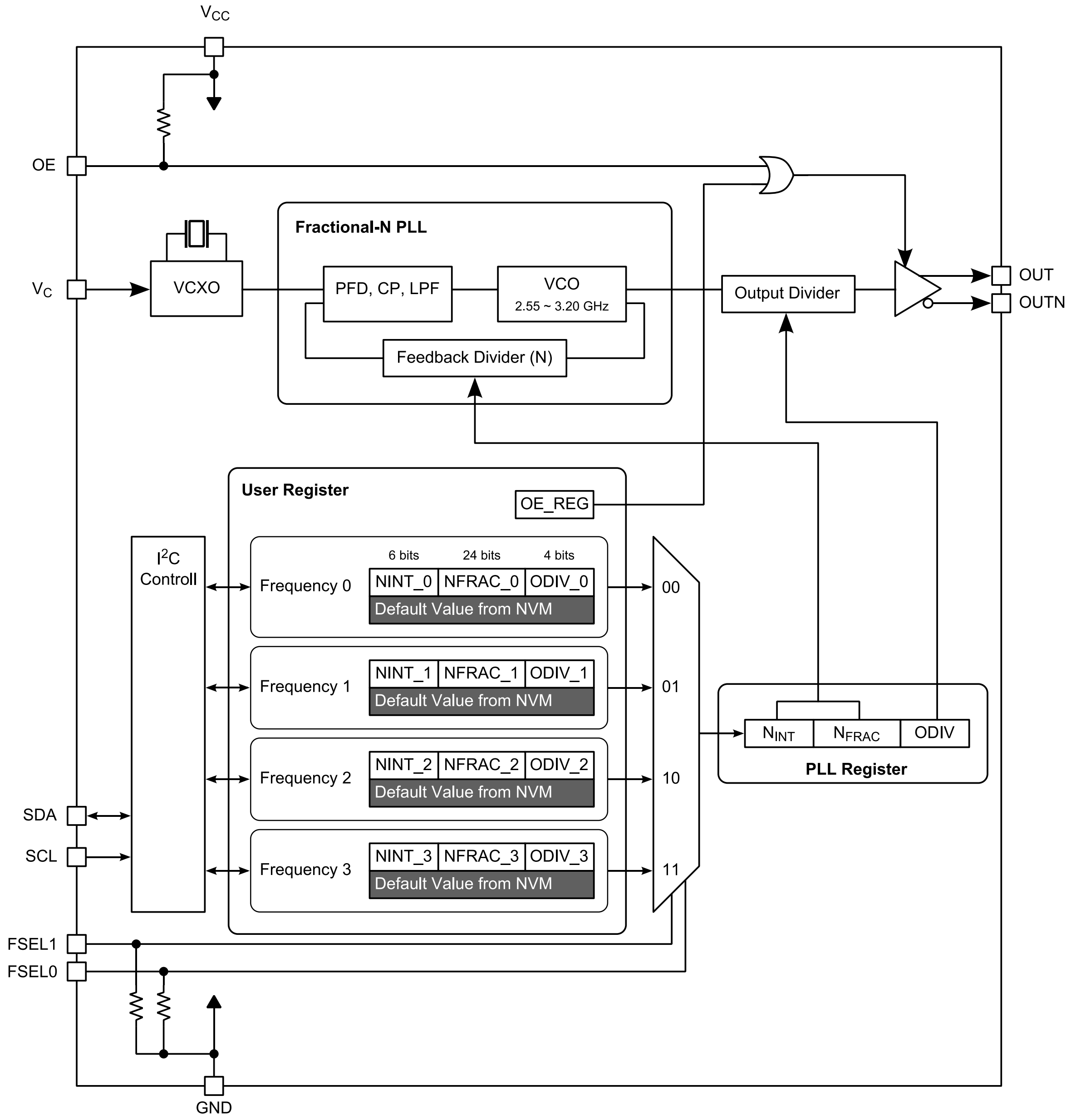
PLL consists of a low jitter fractional-N PLL technology. The components for loop filter are embedded into IC, so no external component is needed.

- Programmable clock output frequency from 50 MHz to 800 MHz
- Frequency setting resolution is around 2 ppb
- Kv is programmable
- Low jitter and high reliability clock source from the fundamental tone internal crystal
- Low jitter and low noise PLL
- Four power-up default frequency
- Factory preset device options
  - OE polarity
  - Output standby type: Hi-Z or OUT = “L”, OUTN = “H”
  - I^2C interface slave address
- Embedded resistors and capacitors for oscillator and loop filter for PLL
- I^2C interface
- LVPECL output
- 10-pin ceramic 5 x 7 mm package
- 2.5 V or 3.3 V supply voltage modes
- -40 °C ~ +85 °C ambient operating temperature
- Pb-free / RoHS-compliant

2. Part Number



3. Block Diagram

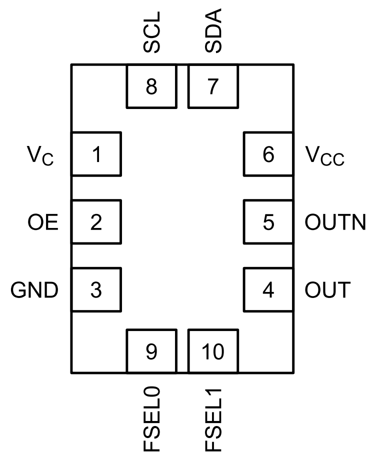


* If OE pin is configured as active low, OE pin is pulled down to GND with internal pull down resistor.

Figure 3.1. VG7050ECN Block Diagram

4. Pin Assignments

4.1. Pin Assignments



(Top View)

4.2. Pin Descriptions

Table 4.1 Pin Descriptions

<table>
<tr><th>No.</th><th>Pin Name</th><th colspan="2">Type</th><th>Function</th></tr>
<tr><td>1</td><td>V_C</td><td>Input</td><td>-</td><td>VCXO Control Voltage Input</td></tr>
<tr><td>2</td><td>OE</td><td>Input</td><td>Pull-up/

Pull-down</td><td>Output Enable (Active High)
<table><tr><td>OE Input</td><td>OUT, OUTN pin status</td></tr><tr><td>“H” or Open</td><td>Outputs are enabled.</td></tr><tr><td>“L”</td><td>High-impedance state
or
OUT = “L”, OUTN = “H”</td></tr></table>
Output Enable (Active Low)
<table><tr><td>OE Input</td><td>OUT, OUTN pin status</td></tr><tr><td>“H”</td><td>High-impedance state
or
OUT = “L”, OUTN = “H”</td></tr><tr><td>“L” or Open</td><td>Outputs are enabled.</td></tr></table></td></tr>
<tr><td>3</td><td>GND</td><td>Power</td><td>-</td><td>Negative Power Supply</td></tr>
<tr><td>4</td><td>OUT</td><td>Output</td><td>-</td><td rowspan="2">Differential clock output. LVPECL interface levels.</td></tr>
<tr><td>5</td><td>OUTN</td><td>Output</td><td>-</td></tr>
<tr><td>6</td><td>V_{CC}</td><td>Power</td><td>-</td><td>Positive Power Supply</td></tr>
<tr><td>7</td><td>SDA*1</td><td>Input/Output</td><td>-</td><td>I²C Data Input/Output
Input: LVCMOS interface levels,
Output: Open drain</td></tr>
<tr><td>8</td><td>SCL*1</td><td>Input</td><td>-</td><td>I²C Clock Input</td></tr>
<tr><td>9</td><td>FSEL0</td><td>Input</td><td>Pull-down</td><td rowspan="2">Frequency select</td></tr>
<tr><td>10</td><td>FSEL1</td><td>Input</td><td>Pull-down</td></tr>
<tr><td colspan="5">Note: “Pull-up” or “Pull-down” refers to VG7050ECN internal input resistors.
*Note 1: External pull-up resistor to V_{CC} is necessary.</td></tr>
</table>

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply voltage, V_{CC}	V_{CC}	GND = 0 V	-0.3	-	4.0	V
Pull-up voltage	V_{PU}	SDA, SCL	-0.3	-	4.0	V
Input voltage 1	V_{in1}	GND = 0 V, Input pins except to SDA and SCL	GND - 0.3	-	V_{CC} + 0.3	V
Input voltage 2	V_{in2}	GND = 0 V, SDA, SCL	GND - 0.3	-	4.0	V
Storage temperature	Tstg	Store as bare product	-55	-	+125	°C
ESD sensitivity	ESD	HBM	2000	-	-	V
		MM	200	-	-	
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed in the “DC characteristics” or “AC characteristics” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.						

5.2. DC Characteristics

Table 5.1. Power Supply, Operating Temperature

GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Positive supply voltage	V_{CC}	3.3 V option	2.970	3.3	3.630	V
		2.5 V option	2.375	2.5	2.625	
Positive supply current[*1] Output enable mode	I_{CC}	OE = Enable, Outputs terminated with 50 Ω to V_{CC} – 2.0 V				
		3.3 V option	-	-	90	mA
		2.5 V option	-	-	90	
Positive supply current[*1] Output disable mode	$I_{\_dis}$	OE = Disable, Output standby type: Hi-Z				
		3.3 V option	-	-	40	mA
		2.5 V option	-	-	40	
		OE = Disable, Output standby type: Fix (OUT = “L”, OUTN = “H”)				
		3.3 V option	-	-	70	mA
		2.5 V option	-	-	70	
Operating temperature	Ta	-	-40	-	+85	°C
Note 1: Guaranteed by design, characterization, and/or simulation only and not production tested.						

Table 5.2. Logic I/O

V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Pull-up voltage	V_{PU}	SDA, SCL	V_{CC} x 0.7	-	3.630	V
High level input voltage 1	V_{IH1}	OE, FSEL0, FSEL1	V_{CC} x 0.7	-	V_{CC} + 0.3	V
High level input voltage 2	V_{IH2}	SDA, SCL, Pull Up Voltage = V_{PU}	V_{CC} x 0.7	-	3.630	V
Low level input voltage	V_{IL}	SDA, SCL, OE, FSEL0, FSEL1	-0.3	-	V_{CC} x 0.3	V
High level input current 1	I_{IH1}	SDA, SCL, OE (Active High) , FSEL0, FSEL1	-	-	2	μA
High level input current 2	I_{IH2}	V_{CC} = 3.3 V ± 10%, OE (Active Low)	-	-	170	μA
		V_{CC} = 2.5 V ± 5%, OE (Active Low)	-	-	100	
Low level input current 1	I_{IL1}	SDA, SCL, OE (Active Low), FSEL0, FSEL1	-2	-	-	μA
Low level input current 2	I_{IL2}	V_{CC} = 3.3 V ± 10%, OE (Active High)	-70	-	-	μA
		V_{CC} = 2.5 V ± 5%, OE (Active High)	-35	-	-	
Low level output voltage	V_{OL}	SDA, at 3 mA sink current	0	-	0.4	V
Low level output current	I_{OL}	SDA, V_{OL} = 0.4 V	3	-	-	mA
Pull-up resistor	R_{UP}	OE (Active High)	-	85	-	kΩ
	R_{DOWN}	OE (Active Low), FSEL0, FSEL1	-	35	-	
Input Capacitance[*1]	C_{IN}	OE, SDA, SCL, FSEL0, FSEL1	-	5	-	pF
Note 1: Guaranteed by design, characterization, and/or simulation only and not production tested.						

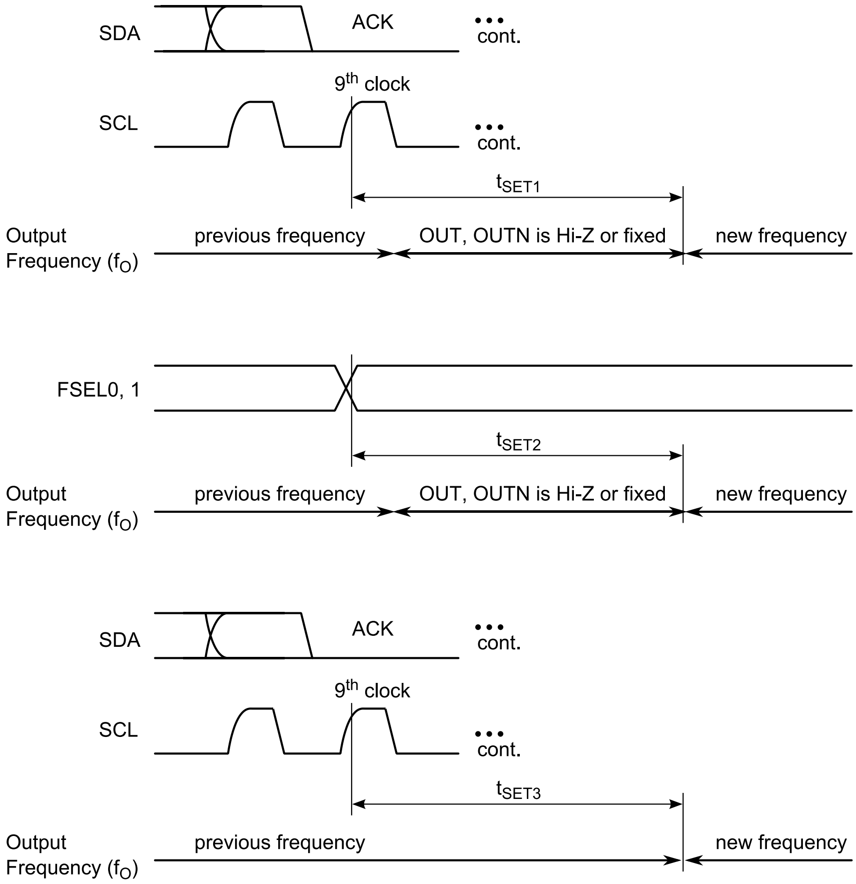
5.3. AC Characteristics

Table 5.3. Output Frequency Characteristics

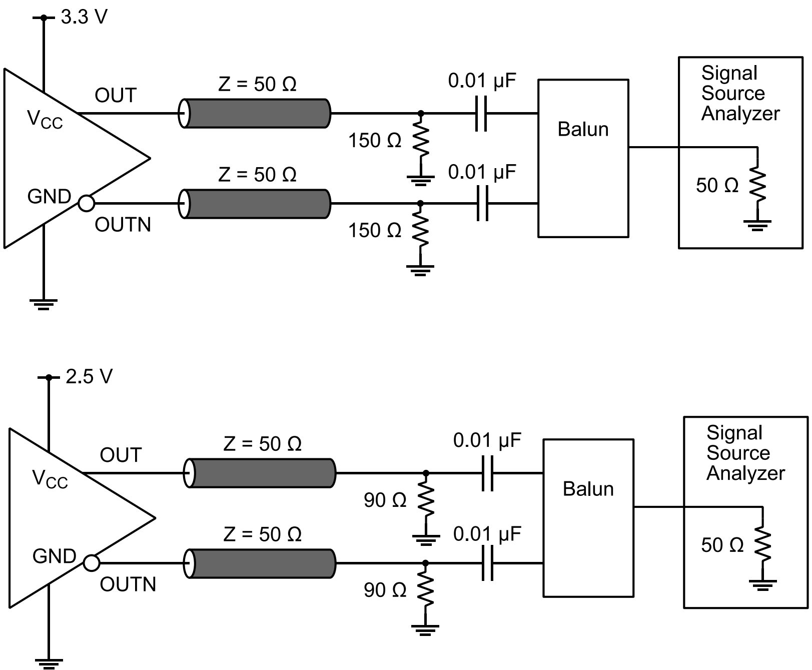
V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Output frequency	f_O	OUT, OUTN	50	-	800	MHz
Internal crystal frequency	f_{XTAL}	-	-	114.144	-	MHz
Frequency reprogramming resolution	M_{RES}	-	2.2	-	2.8	ppb
Frequency tolerance[*1]	f_tol	This parameter includes initial frequency tolerance, temperature, supply voltage variation and 10 years aging[*2] at 25 °C.	-	-	$\pm 50 \times 10^{-6}$	-
Delta frequency for continuous output[*1]	-	From Center Frequency that is defined by setting NEW_FREQ bit	-500	-	500	ppm
Setting time for large frequency change[*1]	t_{SET1}	From setting NEW_FREQ bit to output new frequency	-	-	1.5	ms
Setting time after FSEL0 and FSEL1 values are changed	t_{SET2}	-	-	-	1.5	ms
Setting time for small frequency change[*1]	t_{SET3}	< ±500 ppm from center frequency that is defined by setting NEW_FREQ bit	-	-	100	µs
SSB phase noise[*1]	F_{CN}	f_O = 622.08 MHz, from carrier				
		V_{CC} = 3.3 V[*3], 100 Hz	-	-75.7	-	dBc/Hz
		V_{CC} = 3.3 V[*3], 1 kHz	-	-101.6	-	dBc/Hz
		V_{CC} = 3.3 V[*3], 10 kHz	-	-118.8	-	dBc/Hz
		V_{CC} = 3.3 V[*3], 100 kHz	-	-121.3	-	dBc/Hz
		V_{CC} = 3.3 V[*3], 1 MHz	-	-129.3	-	dBc/Hz
		V_{CC} = 3.3 V[*3], 10 MHz	-	-146.8	-	dBc/Hz
		V_{CC} = 2.5 V[*4], 100 Hz	-	-72.7	-	dBc/Hz
		V_{CC} = 2.5 V[*4], 1 kHz	-	-99.3	-	dBc/Hz
		V_{CC} = 2.5 V[*4], 10 kHz	-	-118.2	-	dBc/Hz
		V_{CC} = 2.5 V[*4], 100 kHz	-	-121.3	-	dBc/Hz
		V_{CC} = 2.5 V[*4], 1 MHz	-	-129.2	-	dBc/Hz
		V_{CC} = 2.5 V[*4], 10 MHz	-	-146.9	-	dBc/Hz
RMS phase jitter[*1, *4]	t_{PJ}	f_O = 622.08 MHz, Integration range: 12 kHz – 20 MHz (OC-48)				
		V_{CC} = 3.3 V[*3]	-	0.3	-	ps
		V_{CC} = 2.5 V[*4]	-	0.3	-	ps
		f_O = 622.08 MHz, Integration range: 20 kHz – 50 MHz				
		V_{CC} = 3.3 V[*3]	-	0.3	-	ps
		V_{CC} = 2.5 V[*4]	-	0.3	-	ps
		f_O = 622.08 MHz, Integration range: 50 kHz – 80 MHz (OC-192)				
		V_{CC} = 3.3 V[*3]	-	0.3	-	ps
		V_{CC} = 2.5 V[*4]	-	0.3	-	ps

Note 1: Guaranteed by design, characterization, and/or simulation only and not production tested.
Note 2: The aging in the frequency tolerance is from environmental tests results to the expectation of the amount of the frequency variation. This doesn't guarantee the product life cycle.
Note 3: f_{XTAL} = 114.144 MHz, Ta = +25 °C, V_{CC} = 3.3 V, V_C = 1.65 V, KV = 0x0.
Note 4: f_{XTAL} = 114.144 MHz, Ta = +25 °C, V_{CC} = 2.5 V, V_C = 1.25 V, KV = 0x0.
Note 5: The output clock may contain spurious that depends on the settings of fo, f_{XTAL}, PLL and output divider. The RMS jitter may be worse, if the spurious is in integration range of RMS jitter. For more information, please contact us.



Frequency Change Time

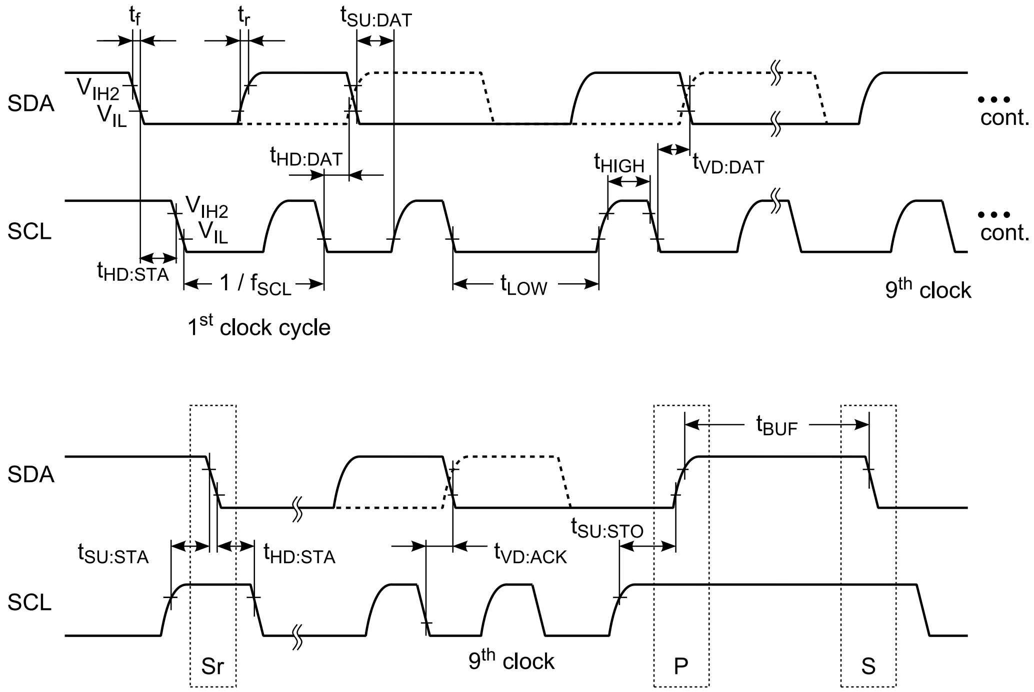


Phase Noise Test Circuit

Table 5.4. Serial Interface

V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL clock frequency	f_{SCL}	-	-	-	400	kHz
Hold time (repeated) START condition, After this period, the first clock pulse is generated.	$t_{HD;STA}$	-	0.6	-	-	μs
Low period of the SCL clock	t_{LOW}	-	1.3	-	-	μs
High period of the SCL clock	t_{HIGH}	-	0.6	-	-	μs
Set up time for a repeated START condition	$t_{SU;STA}$	-	0.6	-	-	μs
Input data hold time	$t_{HD;DAT}$	-	0	-	-	μs
Output data set-up time	$t_{SU;DAT}$	-	100	-	-	ns
Rise time of both SDA and SCL signals*1	t_r	-	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	-	300	ns
Set up time for STOP condition	$t_{SU;STO}$	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t_{BUF}	-	1.3	-	-	μs
Data valid time	$t_{VD:DAT}$	-	-	-	0.9	μs
Data valid acknowledge time	$t_{VD;ACK}$	-	-	-	0.9	μs
Note 1: Guaranteed by design, characterization, and/or simulation only and not production tested.						



Serial Interface

5.4. VCXO Control Voltage Input (V_C)

Table 5.5. VCXO Control Voltage Input (V_C) Characteristics (1)

V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Control voltage tuning range	V_C	-	0	-	V_{CC}	V
V_C input resistance	R_{IN}	DC Level	5	-	-	MΩ
Nominal Control Voltage	VC_{NOM}	V_{CC} = 3.3 V ± 10%	-	1.65	-	V
		V_{CC} = 2.5 V ± 5%	-	1.25	-	
Frequency Change Polarity		-	Positive slope			-

Table 5.6. VCXO Control Voltage Input (V_C) Characteristics (2)

V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions		Min.	Typ.	Max	Units
Control voltage linearity	f_lin	BSL	V_{CC} = 3.3 V, V_C = 0.3 V ~ 3.0 V	-	-	±10	%
			V_{CC} = 2.5 V, V_C = 0.25 V ~ 2.25 V	-	-	±10	
Modulation bandwidth	BW	±3 dB, reference input: 1 kHz		10	-	-	kHz
Absolute pull range [*1]	APR	V_{CC} = 3.3 V, V_C = 0.3 V ~ 3.0 V, f_{XTAL} = 114.144 MHz	KV Register				
			0x0	180	-	-	ppm
			0x1	164	-	-	
			0x2	148	-	-	
			0x3	132	-	-	
			0x4	116	-	-	
			0x5	99	-	-	
			0x6	83	-	-	
			0x7	67	-	-	
			0x8	51	-	-	
			0x9	35	-	-	
			0xA	19	-	-	
			0xB	3	-	-	
		V_{CC} = 2.5 V, V_C = 0.25 V ~ 2.25 V, f_{XTAL} = 114.144 MHz	KV Register				
			0x0	183	-	-	ppm
			0x1	166	-	-	
			0x2	150	-	-	
			0x3	134	-	-	
			0x4	118	-	-	
			0x5	102	-	-	
			0x6	86	-	-	
			0x7	69	-	-	
			0x8	54	-	-	
			0x9	38	-	-	
			0xA	22	-	-	
			0xB	6	-	-	
Note: Guaranteed by design, characterization, and/or simulation only and not production tested.							

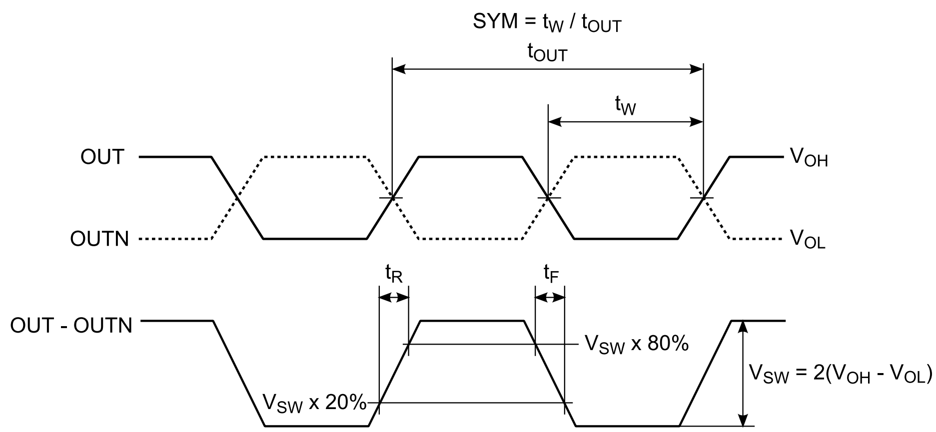
5.5. LVPECL

Table 5.7. LVPECL

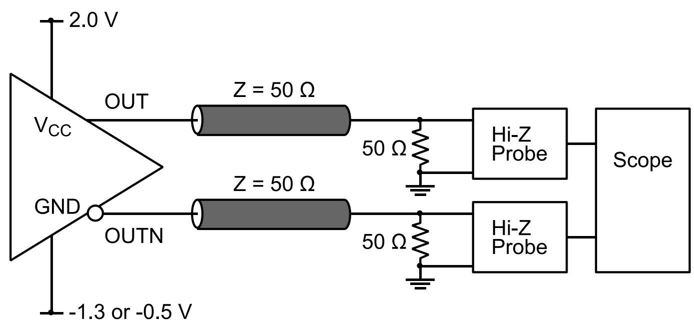
V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max	Units
Output load condition	L_PECL	Outputs terminated with 50 Ω to V_{CC} – 2.0 V				-
Rise time*1	t_R	-	-	-	400	ps
Fall time*1	t_F	-	-	-	400	ps
Symmetry*1 (duty cycle)	SYM	-	45	50	55	%
High level output voltage	V_{OH}	-	V_{CC} – 1.025	V_{CC} – 0.95	-	V
Low level output voltage	V_{OL}	-	-	V_{CC} – 1.7	V_{CC} – 1.62	V
OE disable delay time*1	t_{PXZ}	-	-	-	100	ns
OE enable delay time*1	t_{pZX}	-	-	-	10	μs

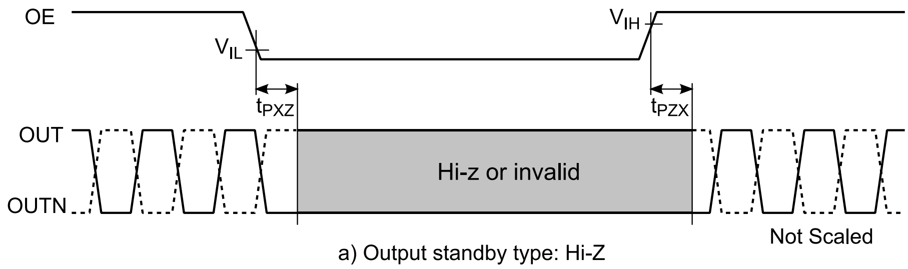
Note: OUT and OUTN are not used as single end.
Note 1: Guaranteed by design, characterization, and/or simulation only and not production tested.



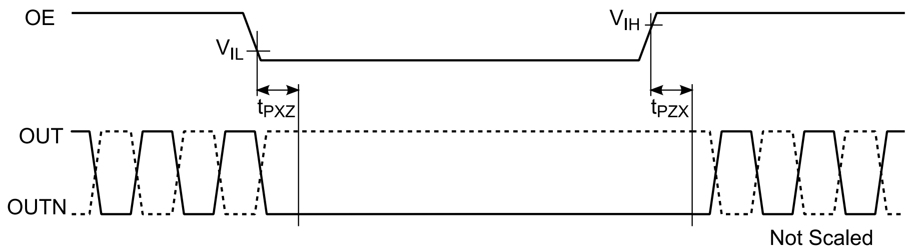
Output Rise/Fall Time, Symmetry (duty cycle)



Output AC Test Circuit



a) Output standby type: Hi-Z



b) Output standby type: Fix

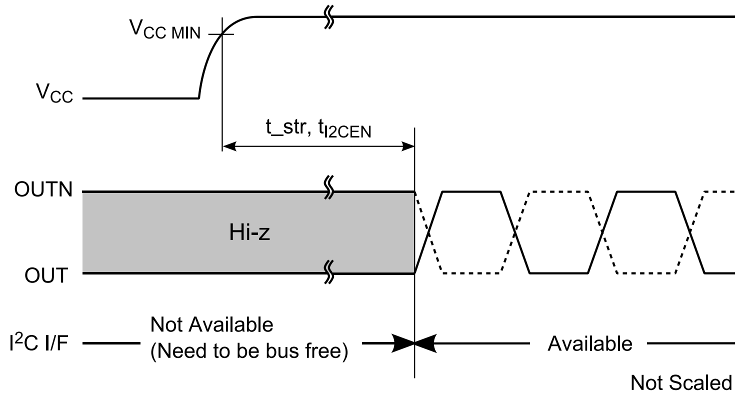
OE function (Active High)

5.6. Startup

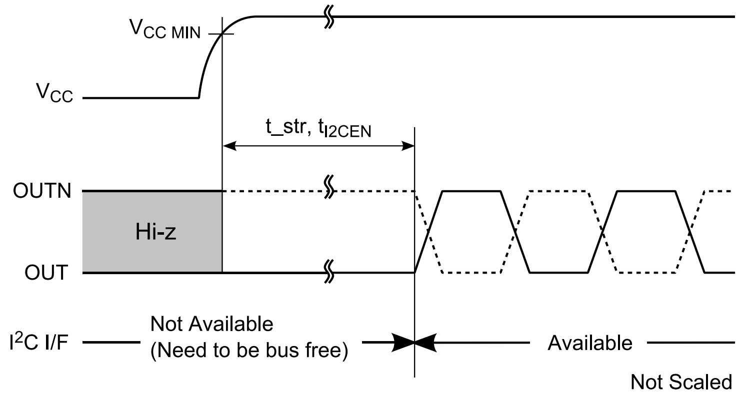
Table 5.8. Startup

V_{CC} = 3.3 V ± 10% or 2.5 V ± 5%, GND = 0 V, Ta = -40 ~ +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max	Units
V_{CC} ramp rate[*1]	R_{VCC}	V_{CC} from 0 V to $V_{CC\ MIN}$.	5×10^{-6}	-	3	s
Startup time[*2]	t_str	-	-	-	5	ms
I^2C I/F enable time[*2]	t_{I2CEN}	-	-	-	5	ms
Note 1: V_{CC} ramp must be monotonic. Note 2: Guaranteed by design, characterization, and/or simulation only and not production tested.						



a) Output standby type: Hi-Z



b) Output standby type: Fix

Start-Up Time

6. Functions

6.1. Overview

The VG7050ECN has a VCXO, PLL and output buffer unit. The VCXO unit is composed of a fundamental mode crystal that generates stable reference clock for PLL. Kv of VCXO can be programmed via I^2C interface. For best phase noise performance, Kv can be selected the lowest setting that meets the requirements of the application. The output frequency is determined by the feedback divider and the output divider. The feedback divider can offer not only integer setting that achieves lower jitter, but also fractional setting that provides frequency in ppb resolution.

The device's default output frequency and Kv are set at the factory and can be reprogrammed via I^2C bus. Once the device is powered down, it will return to its factory-set default setting.

6.2. Setting of the Kv

The VG7050ECN has Voltage Control function in its crystal oscillation circuit. The Kv value, pull range sensitivity of the V_C function, is the factory default value when the device is powered on. It can be reprogrammed by setting the KV.KV register through I^2C bus.

Table 6.1. Setting of the Kv

Register	Setting	Kv *
KV.KV	0xC ~ 0xF	Forbidden
	0xB	Min
	…	…
	0x0	Max

***Please refer to the Kv values for the Table 5.6**

6.3. Setting of the Output Frequency

6.3.1. Calculation of the Frequency Setting

The output frequency (f_O) is determined by the VCO frequency (f_{VCO}) and the output divider (ODIV). This is shown:

$$f_O = \frac{f_{VCO}}{ODIV} \tag{1}$$

The VCO frequency must be from 2.55 GHz to 3.20 GHz. Base on the relation between this limit and the formula (1), ODIV is calculated from the f_O as shown in Table 6.2.

The VCO frequency is determined by the reference frequency (f_{REF}) from the VCXO and the feedback divider (N). The feedback divider (N) consists of both a 6-bit integer portion (N_{INT}) and a 24-bit fractional portion (N_{FRAC}) and provides the means for high-resolution frequency generation. The VCO frequency is calculated by:

$$\begin{aligned} f_{VCO} &= f_{REF} \times N \\ &= f_{REF} \times \left(N_{INT} + \frac{N_{FRAC}}{2^{24}}\right) \end{aligned} \tag{2}$$

Table 6.2. f_O and ODIV

f_O [MHz]	ODIV	ODIV.ODIV register setting
50 ~ 57	56	0xF
53 ~ 67	48	0xE
64 ~ 80	40	0xD
80 ~ 100	32	0xC
91 ~ 114	28	0xB
106 ~ 133	24	0xA
128 ~ 160	20	0x9
159 ~ 200	16	0x8
182 ~ 229	14	0x7
213 ~ 267	12	0x6
255 ~ 320	10	0x5
319 ~ 400	8	0x4
364 ~ 457	7	0x3
425 ~ 533	6	0x2
510 ~ 640	5	0x1
638 ~ 800	4	0x0

The output frequency (f_O) is shown:

$$\begin{aligned} f_O &= \frac{f_{VCO}}{ODIV} \\ &= f_{REF}\frac{\left(N_{INT} + \frac{N_{FRAC}}{2^{24}}\right)}{ODIV} \end{aligned}$$

(3)

For example if the reference frequency (f_{REF}) is 114.144 MHz and the output frequency is 120MHz, ODIV is fixed to “24” from the Table 6.2. The setting of N, N_{INT}, N_{FRAC} is calculated:

$$N = N_{INT} + \frac{N_{FRAC}}{2^{24}} = \frac{f_{OUT} \times ODIV}{f_{REF}} = \frac{120.0 \times 10^6 \times 24}{114.1444444 \times 10^6} = 25.231188535690308$$

(4)

$$N_{INT} = floor(N) = floor(25.231188535690308) = 25$$

(5)

$$\begin{aligned} N_{FRAC} = (N - N_{int}) \times 2^{24} &= (25.231188535690308 - 25) \times 2^{24} \\ &= 0.231188535690308 \times 2^{24} \\ &\cong 3878700 = 0x3B2F2C \end{aligned}$$

(6)

Depending on the fo, the ODIV may become two values.

For example if the fo is 380 MHz, ODIV can be 7 or 8. Even if either of the ODIV values is selected, the same fo can be gained by setting NINT and NFRAC but phase noise included in the output signal become different. Please evaluate the performances fully in your actual usage environment and select the ODIV.

N_{FRAC} is a 24-bit value. By setting 6 bit of N_{INT} and 20 bit of N_{INT} frequency resolution is 10 ppb order. The lower 4 bit of the rest of the N_{FRAC} corresponds to the setting of the frequency in 1ppb order. By setting these values, the output frequency is changed very small, but the spurious of the output signal may change significantly. Please evaluate the performances fully in your actual usage environment and fix the lower 4 bit of the N_{FRAC}.

6.3.2. **Reconfiguring Frequency Setting**

The VG7050ECN has four sets of "user register", “user register selector” and a "PLL register". The user register stores ODIV, NINT and NFRAC. It can be reprogrammed at any time when I^2C bus is available. The user resister selector is controlled by FSEL0 and FSEL1 pins. It selects one frequency settings (ODIV, NINT and NFRAC) from the four sets of user register. The PLL register is connected directly to the PLL.

When the device is powered on, the default value programmed in the non-volatile memory is automatically fetched to the four sets of user register. The user register selector selects frequency settings from them, and then it is loaded by the PLL register.

After power up, the user may change output frequency selection from the factory programmed four frequency by changing FSEL0 and FSEL1 pins. When VG7050ECN detect the change of FSEL0 and FSEL1 pins, clock output momentary stops. The, the PLL register is updated by the user register selected by FSEL0 and FSEL1 pins, PLL calibration is executed, and then clock output resumes at new frequency.

Table 6.3 Frequency selection by FSEL0 and FSEL1 pins

Input		Frequency Select	User Register
FSEL1	FSEL0		
0	0	Frequency 0	ODIV0, NINT0, NFRAC_H0, NFRAC_M0, NFRAC_L0
0	1	Frequency 1	ODIV1, NINT1, NFRAC_H1, NFRAC_M1, NFRAC_L1
1	0	Frequency 2	ODIV2, NINT2, NFRAC_H2, NFRAC_M2, NFRAC_L2
1	1	Frequency 3	ODIV3, NINT3, NFRAC_H3, NFRAC_M3, NFRAC_L3

The user may change output frequency different than that programmed by the factory. VG7050ECN has two frequency change method, a) clock stops momently and PLL calibration, b) clock output continuously and no PLL calibration. With method “a”, new output frequency can be set as any frequency. With method “b”, the change of output frequency is limited within ±500 ppm.

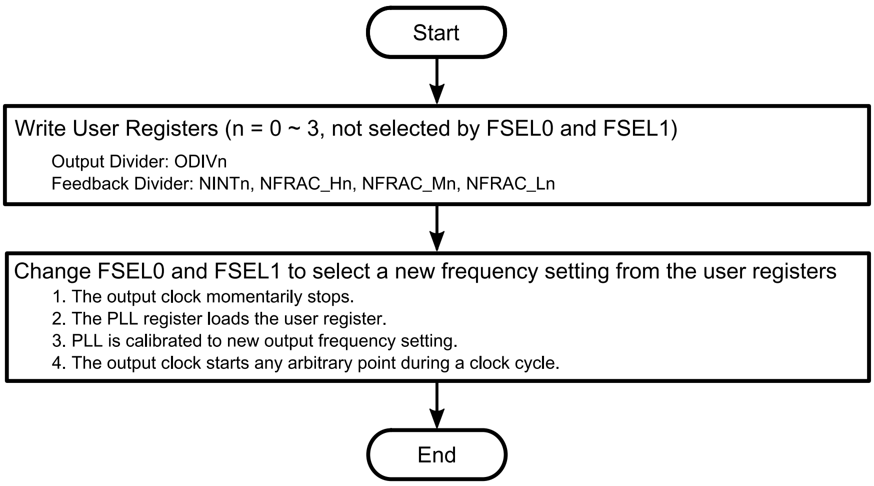
6.3.2.1. Output Frequency Change to Any Frequency with PLL Calibration

The frequency change procedure is shown in **Figure 6.1**.

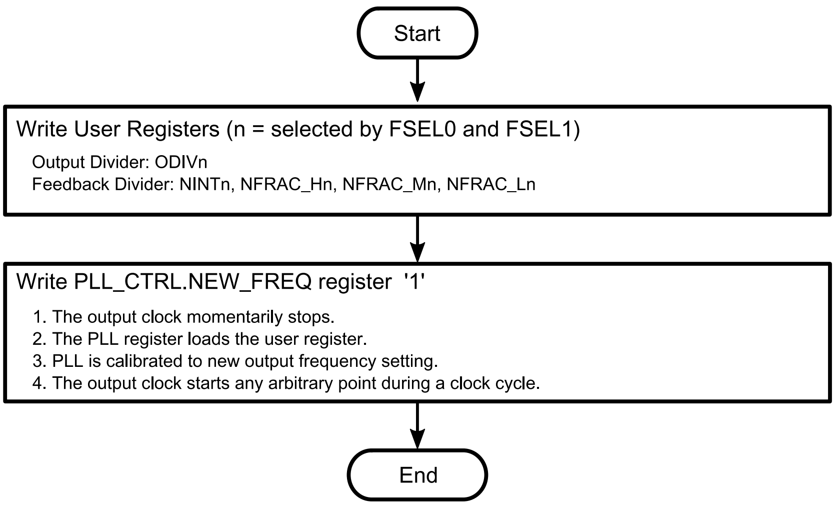
If the user write a different ODIVn, NINTn, NFRAC_Hn, NFRAC_Mn, NFRAC_Ln; n = 0, 1, 2 or 3, the user writes to a configuration which is not currently selected by FSEL0 and FSEL1 pins and then change to that configuration after the I^2C transaction has completed. Changing the FSEL0 and FSEL 1 pins controls results in an immediate output clock halt, PLL calibration, and then output clock resumes at new frequency.

If FSEL0 and FSEL1 pins are fixed, the user writes to a configuration which is currently selected by FSEL0 and FSEL1 pins, and writes 1 to the PLL_CTRL.NEW_FREQ register. It also results in an immediate output clock halt, PLL calibration, and then output clock resumes at new frequency.

Both method results in PLL calibration for new output frequency, optimum jitter performance is achieved. These methods establish a new center frequency. Circuitry receiving a clock from the VG7050ECN that is sensitive to glitches or runt pulses may have to be reset once this process is complete.



a) Change a frequency setting and select it by FSEL0, FSEL1



b) Change a frequency setting and request to load it

Figure 6.1 Frequency change procedure with PLL calibration

6.3.2.2. Output Frequency Small Change without PLL Calibration

The user may change output frequency without clock pause. With this method, PLL calibration is not executed and frequency change window is limited within ±500 ppm from the center frequency as shown in Figure 6.2

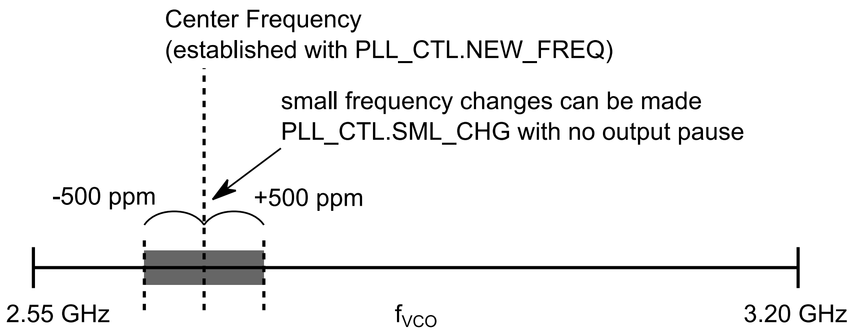


Figure 6.2 VCO frequency range

Frequency change procedure is shown in Figure 6.3. The user may write new frequency settings to the user resister (NINT, NFRAC only) which is selected by FSEL0 and FSEL1 pins, and then the user write 1 to the PLL_CTRL.SML_CHG register. It results in a change of output frequency without clock output pause.

PLL calibration is not preceded in this method; therefore the jitter performance may not be optimum. During output frequency change, the output frequency might temporarily be outside the frequency band between old frequency and new frequency.

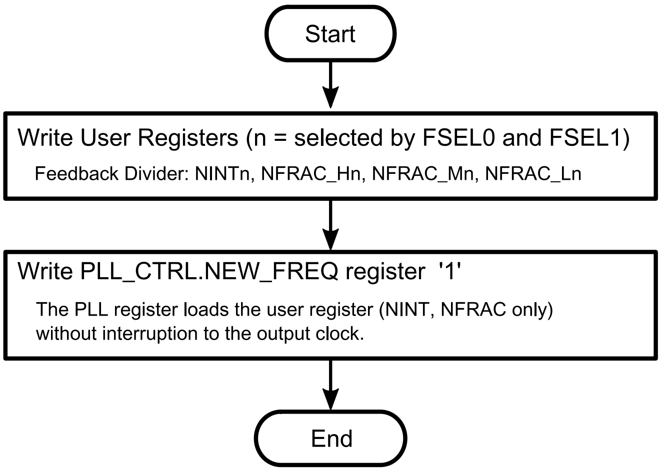


Figure 6.3 Frequency change procedure without PLL calibration

6.4. I^2C Interface

6.4.1. **Connection of I^2C Bus**

The VG7050ECN can be used as a slave device of I^2C bus. The I^2C bus is composed of serial data line (SDA) and serial clock (SCL). The lines need to be both pulled up by external resistors. Electric level of the pull up resistor need to be above the Vcc so these are recommended to be pulled up to the Vcc. Also slave address of the slave devices on the I^2C bus must be unique.

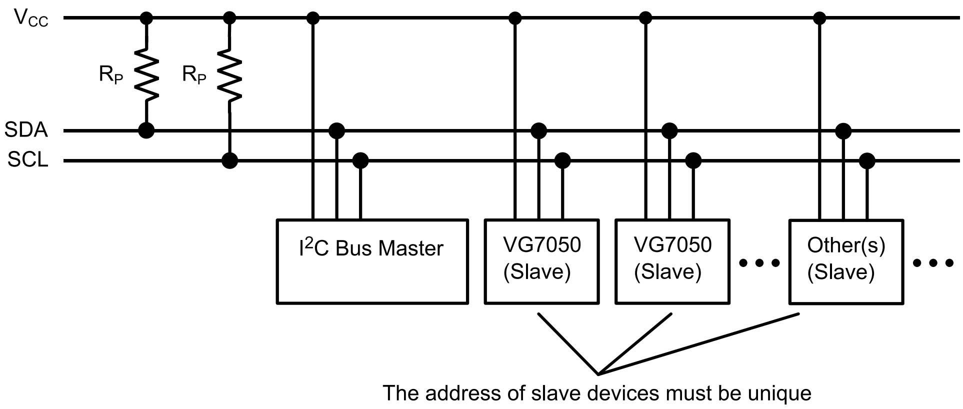


Figure 6.4. Connection of I^2C bus

6.4.2. I²C Bus Protocols Supported by the VG7050ECN

I2C bus protocols that can be supported by the VG7050ECN are shown in the below Table 6.4.

Table 6.4. I²C bus protocols supported by the VG7050ECN

Feature	VG7050ECN
START condition	✓
STOP condition	✓
Acknowledge	✓
Clock stretching	n/a
7-bit slave address	✓
10-bit slave address	n/a
General Call address	n/a
Software Reset	n/a
Device ID	n/a

n/a = not applicable

6.4.3. START Condition and STOP Condition

Data communication on the I²C bus starts by START condition (S). The START condition means that SDA changes from "H" to "L" when SCL is at "H". When the START condition occurs, I²C bus becomes busy.

Data communication on the I²C bus can be terminated by STOP condition (P). The STOP condition means that SDA changes from "L" to "H" when SCL is at "H". When the STOP condition occurs, I²C bus becomes free.

When I²C bus is busy, instead of STOP condition START condition can be generated, which is called repeated START condition (Sr). The I²C bus maintains busy status. If the START or repeated START condition is received, I²C interface circuit of the VG7050ECN is always reset, even if these START conditions are not positioned according to the proper format.

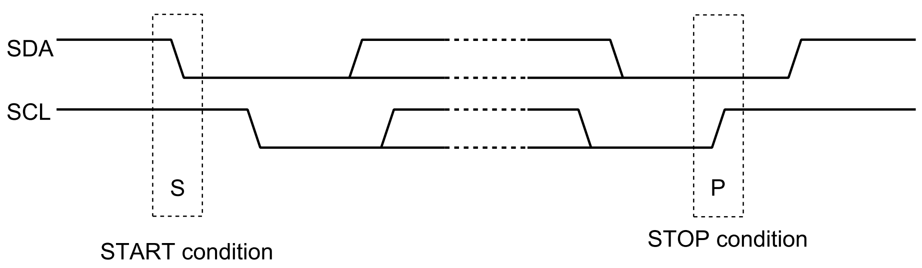


Figure 6.5. START and STOP condition

6.4.4. **Byte Format and ACK/NACK**

Data transmission and reception on I^2C is done in a unit of 8 bit = 1 byte. Each byte is followed by acknowledge bit. Data is transmitted by MSB first. Including acknowledge bit all SCL pulses are generated by Master.

The Acknowledge signal (ACK: A) is defined as follows: the transmitter (master transmitter or slave transmitter) releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line "L" and it remains stable "L" during the "H" period of this clock pulse. When SDA remains "H" during this ninth clock pulse, this is defined as the Not Acknowledge signal (NACK: $\overline{A}$).

6.4.5. **Read/Write to Register**

Procedure of Read/Write to register is shown in the below Figure 6.6. The VG7050ECN can Read/Write single or multi byte data. The VG7050ECN slave address is 0x37.

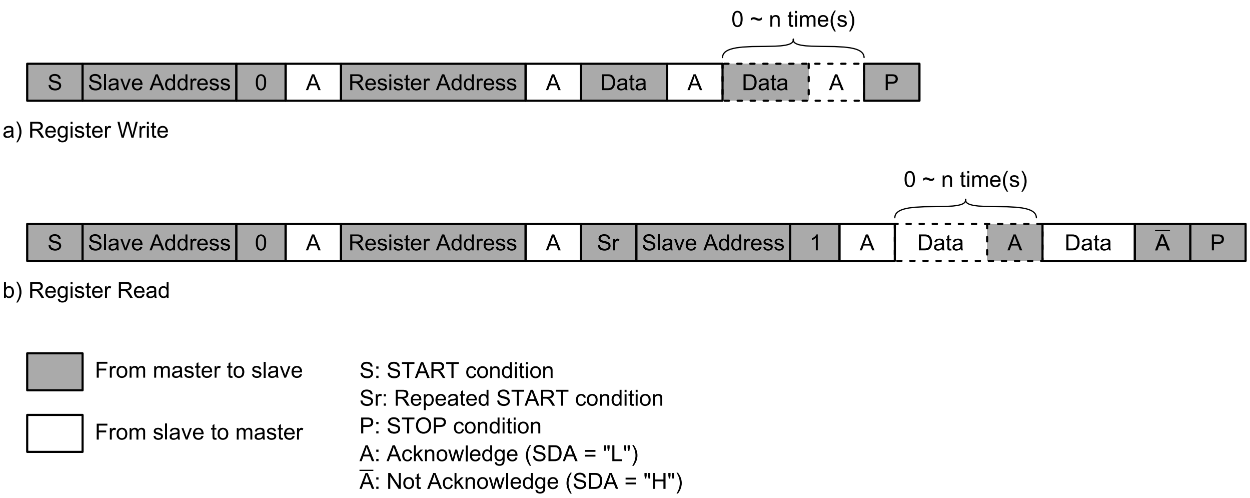


Figure 6.6. Read/Write from/to register by I^2C bus

7. Registers

7.1. List of Registers

Address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	P_CODE0	0x46 (Ascii 'F', Read Only)							
0x01	P_CODE1	0x43 (Ascii 'C', Read Only)							
0x02	REV	0x01 (Read Only)							
0x03	ID_CODE0	0x01 (Read Only)							
0x04	ID_CODE1	-	ID (Read Only)						
0x10	ODIV0	-	-	-	-	ODIV			
0x11	NINT0	-	-	NINT					
0x12	NFRAC_H0	NFRAC_H							
0x13	NFRAC_M0	NFRAC_M							
0x14	NFRAC_L0	NFRAC_L							
0x15	PLL_CTRL0	OE_REG	-	-	-	VCTUNE_DIS	NEW_FREQ	SML_CHG	NVM_RESTORE
0x16	FSEL_STAT0	-	-	-	-	-	-	FSEL (Read Only)	
0x20	ODIV1	-	-	-	-	ODIV			
0x21	NINT1	-	-	NINT					
0x22	NFRAC_H1	NFRAC_H							
0x23	NFRAC_M1	NFRAC_M							
0x24	NFRAC_L1	NFRAC_L							
0x30	ODIV2	-	-	-	-	ODIV			
0x31	NINT2	-	-	NINT					
0x32	NFRAC_H2	NFRAC_H							
0x33	NFRAC_M2	NFRAC_M							
0x34	NFRAC_L2	NFRAC_L							
0x40	ODIV3	-	-	-	-	ODIV			
0x41	NINT3	-	-	NINT					
0x42	NFRAC_H3	NFRAC_H							
0x43	NFRAC_M3	NFRAC_M							
0x44	NFRAC_L3	NFRAC_L							
0x50	PLL_CTRL1	OE_REG	-	-	-	VCTUNE_DIS	NEW_FREQ	SML_CHG	NVM_RESTORE
0x51	FSEL_STAT1	-	-	-	-	-	-	FSEL (Read Only)	
0x5A	KV	-	-	-	-	KV			

Note: Please do not write values in the addresses that are not mentioned in this list. Please write 0 in the bit that is not defined.

7.2. Product Code 0 Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	P_CODE0	P_CODE							
Type		R/O							
Default		0	1	0	0	0	1	1	0

Bit	Name	Function
7:0	P_CODE	**Product code (0x46)** Ascii Code 'F'

7.3. Product Code 1 Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	P_CODE1	P_CODE							
Type		R/O							
Default		0	1	0	0	0	0	1	1

Bit	Name	Function
7:0	P_CODE	**Product code (0x43)** Ascii Code 'C'

7.4. Revision Code Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	REV	REV							
Type		R/O							
Default		0	0	0	0	0	0	0	1

Bit	Name	Function
7:0	REV	**Revision code** 0x01

7.5. ID Code 0 Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	ID_CODE0	ID							
Type		R/O							
Default		0	0	0	0	0	0	0	1

Bit	Name	Function
7:0	ID	**ID code** 0x01

7.6. ID Code 1 Register

Address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	ID_CODE1	-	ID						
Type		-	R/O						
Default		-	Depend on the product						

Bit	Name	Function
7	Reserved	Always read as 0.
6:0	ID	**ID code** Lower 7 bit value of the parameter designator (SM20xxxx)

7.7. ODIV Register

Address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	ODIV0	-	-	-	-	ODIV			
0x20	ODIV1								
0x30	ODIV2								
0x40	ODIV3								
Type		-	-	-	-	R/W			
Default		-	-	-	-	NVM			

Bit	Name	Function
7:4	Reserved	Please write 0 at all the times.
3:0	ODIV	**Division ratio of output divider**

0x0: 4	0x4: 8	0x8: 16	0xC: 32
0x1: 5	0x5: 10	0x9: 20	0xD: 40
0x2: 6	0x6: 12	0xA: 24	0xE: 48
0x3: 7	0x7: 14	0xB: 28	0xF: 56

7.8. NINT Register

Address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	NINT0	-	-	NINT					
0x21	NINT1								
0x31	NINT2								
0x41	NINT3								
Type		-	-	R/W					
Default		-	-	NVM					

Bit	Name	Function
7:6	Reserved	Please write 0 at all the times.
5:0	NINT	**Integer portion of the feedback divider (N_{INT})**

Setting		Description
0x00 ~ 0x11,	0d ~ 17d	This setting shall not be configured.
0x12	18d	N_{INT} = 18
...	...	...
0x20	32d	N_{INT} = 32
0x21 ~ 0x3F	33d ~ 63d	This setting shall not be configured.

7.9. NFRAC Register

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	NFRAC_H0	NFRAC[23:16]							
0x22	NFRAC_H1								
0x32	NFRAC_H2								
0x42	NFRAC_H3								
0x13	NFRAC_M0	NFRAC[15:8]							
0x23	NFRAC_M1								
0x33	NFRAC_M2								
0x43	NFRAC_M3								
0x14	NFRAC_L0	NFRAC[7:0]							
0x24	NFRAC_L1								
0x34	NFRAC_L2								
0x44	NFRAC_L3								
Type		R/W							
Default		NVM							

Bit	Name	Function
7:0	NFRAC[23:16] NFRAC[15:8] NFRAC[7:0]	**Fractional portion of the feedback divider (N_{FRAC})** E.g. Setting in case N_{FRAC} is 0x123456 NFRAC_H = 0x12 NFRAC_M = 0x34 NFRAC_L = 0x56

7.10. PLL Control Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15 0x50	PLL_CTRL0 PLL_CTRL1	OE_REG	-	-	-	VCTUNE_DIS	NEW_FREQ	SML_CHG	NVM_RESTORE
Type		R/W	-	-	-	R/W	R/W	R/W	R/W
Default		0	-	-	-	0	0	0	0

PLL_CTRL0 and PLL_CTRL1 is an address shared register.

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>7</td><td>OE_REG</td><td>Output enable register function
LVPECL output buffer is enable when OE pin or this register is set as 1/High as shown below table.

LVPECL output buffer
<table>
<tr><td></td><td></td><td colspan="2">OE pin (Active High) status</td><td colspan="2">OE pin (Active Low) status</td></tr>
<tr><td></td><td></td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td rowspan="2">OE_REG value</td><td>1</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>0</td><td>Enable</td><td>Disable</td><td>Disable</td><td>Enable</td></tr>
</table>
</td></tr>
<tr><td>6:4</td><td>Reserved</td><td>Please write 0 at all the times.</td></tr>
<tr><td>3</td><td>VCTUNE_DIS</td><td>VC function (VCXO)
0: VC function is valid
1: VC function is invalid</td></tr>
<tr><td>2</td><td>NEW_FREQ</td><td>New frequency applied
By writing 1, frequency setting configured in user register is forwarded to PLL register and output frequency is updated accordingly. This bit is automatically cleared once change of the output frequency and PLL calibration is completed.

Note: Please refer to the item 6.3.2 for details of frequency change by this bit.</td></tr>
<tr><td>1</td><td>SML_CHG</td><td>New frequency applied (small change in frequency)
By writing 1, frequency setting configured in user register is forwarded to PLL register and output frequency is updated accordingly. This bit is automatically cleared once change of the output frequency is done.

Note: Please refer to the item 6.3.2 for details of frequency change by this bit.</td></tr>
<tr><td>0</td><td>NVM_RESTORE</td><td>Restore user register from NVM
By writing 1, default value of user register is restored from non-volatile memory (NVM). This bit is automatically cleared once the register restore is done.

Note: PLL register is not updated only by writing to this bit. In order to initialize the user register and the PLL register (= output frequency) at the same time, please write 0x05 to PLL_CTRL register (NEW_FREQ bit and NVM_RESTORE bit is written as 1).</td></tr>
</table>

7.11. FSEL Status Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	FSEL_STAT0	-	-	-	-	-	-	FSEL	
0x52	FSEL_STAT1								
Type		-	-	-	-	-	-	R/O	
Default		-	-	-	-	-	-	-	

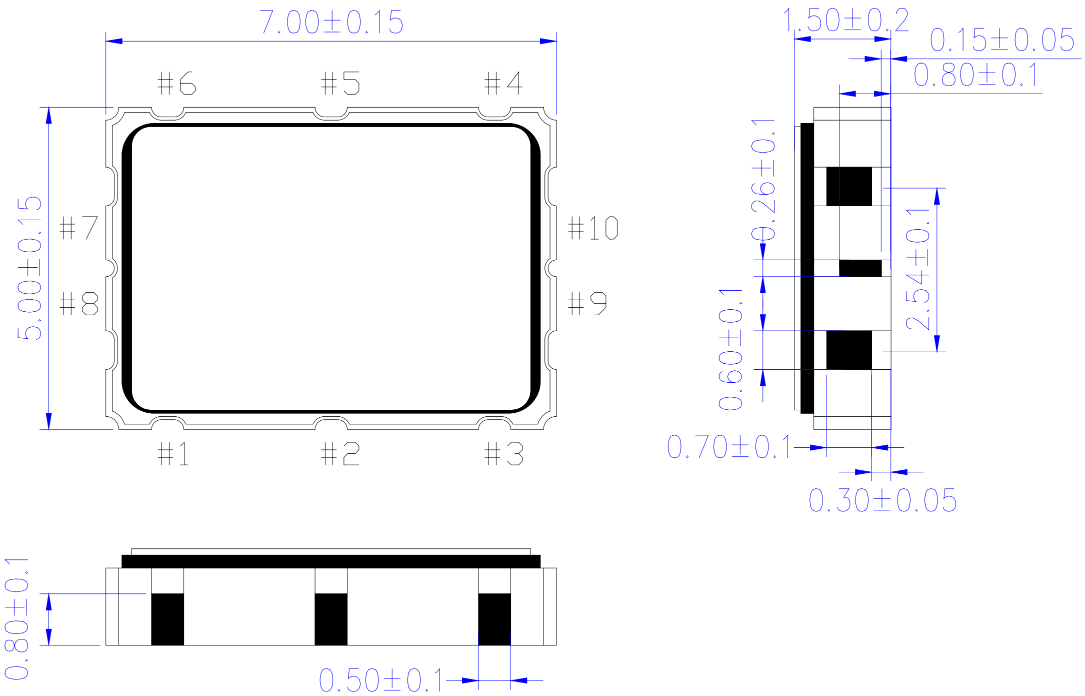
Bit	Name	Function
7:2	Reserved	Please write 0 at all the times.
1:0	FSEL	**FSEL0, FSEL1 settings** This register shows the current number of frequency selection (0 ~ 3). If FSEL0 or FSEL1 pin is changed, it is not updated immediately. After t_{SET2}, VG7050ECN outputs new frequency and this resister is updated.

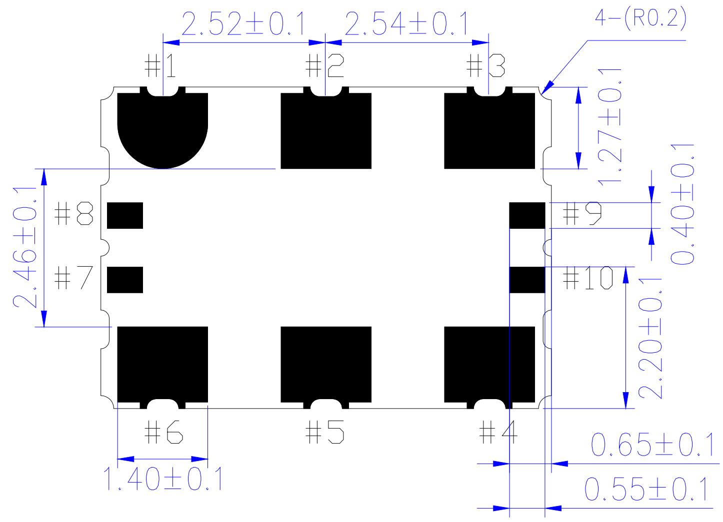
7.12. KV Register

Address	Register name	Bit							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5A	KV	-	-	-	-	KV			
Type		-	-	-	-	R/W			
Default		-	-	-	-	NVM			

Bit	Name	Function
7:4	Reserved	Please write 0 at all the times.
3:0	KV	**Kv setting of VCXO** Please refer to electrical characteristics spec (Table 5.6) for relation between setting and Kv.

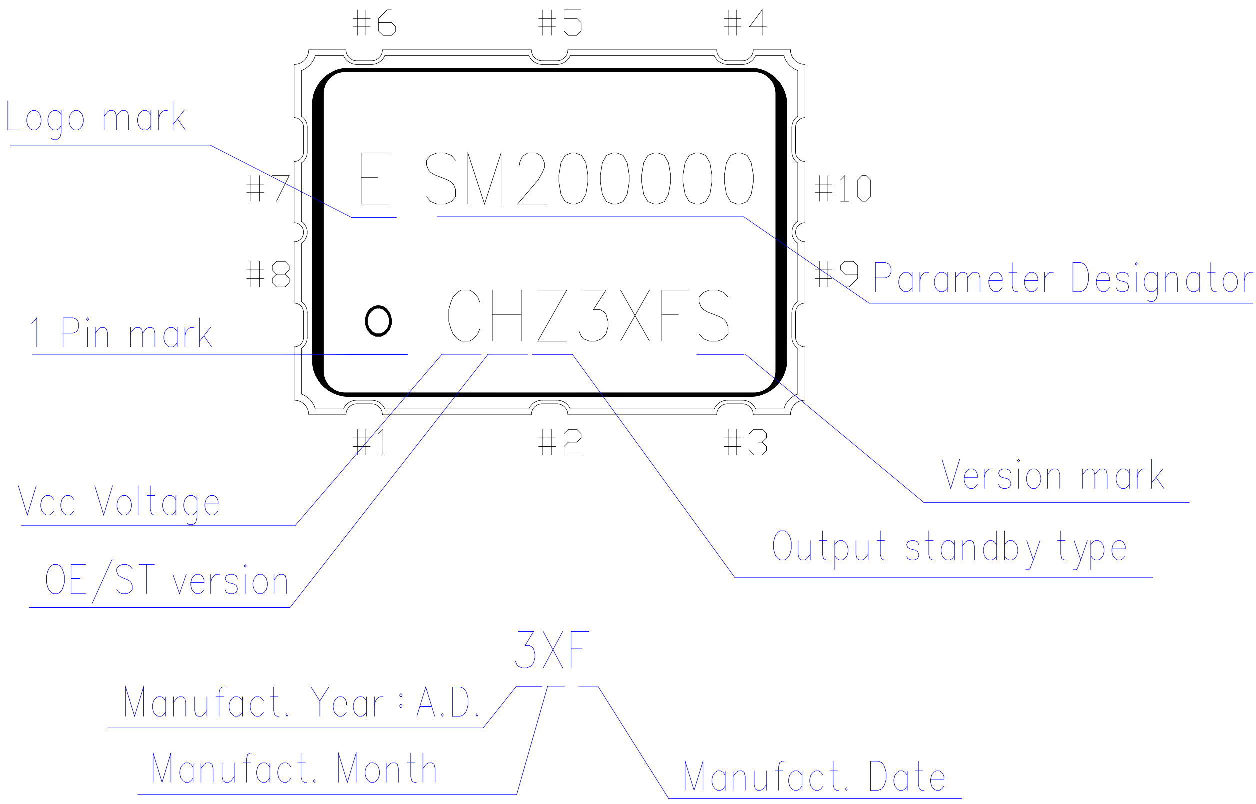
8. Dimensions





No	Pin Name
#1	Vc
#2	OE
#3	GND
#4	OUT
#5	OUTN
#6	Vcc
#7	SDA
#8	SCL
#9	FSEL0
#10	FSEL1

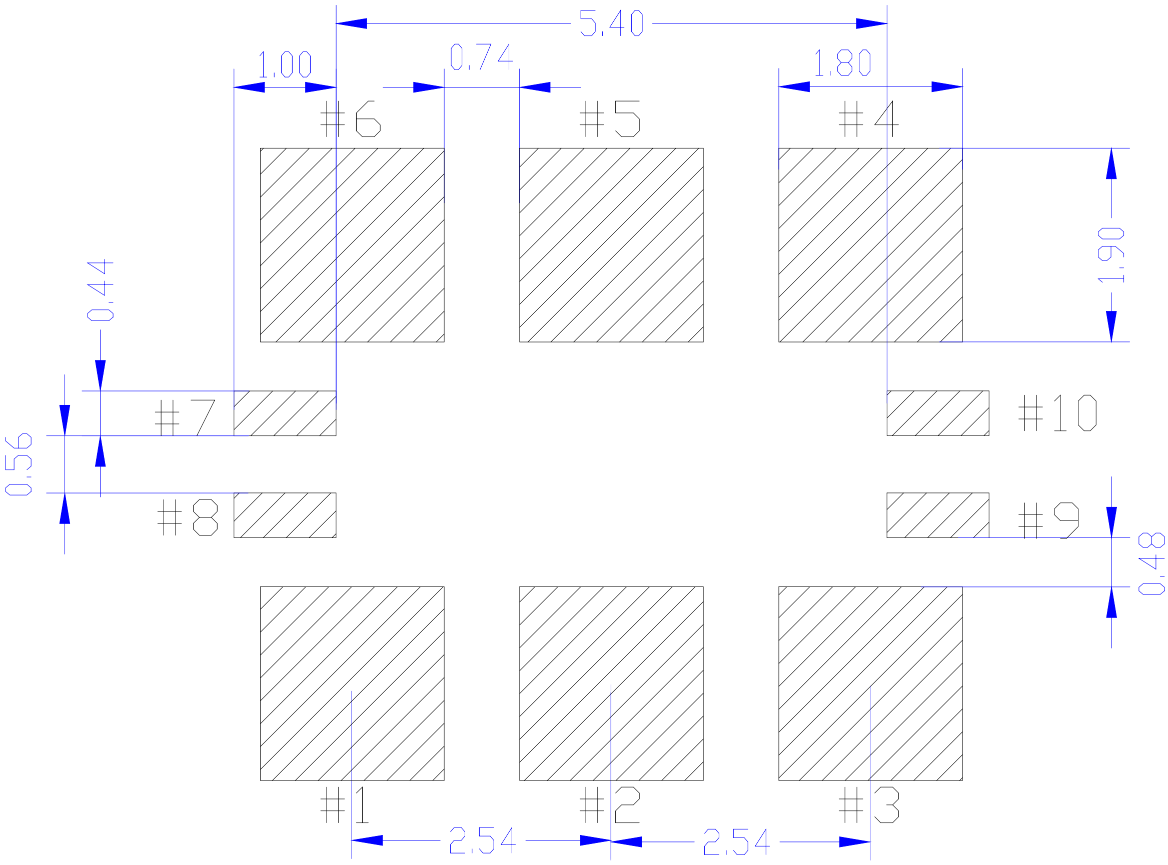
9. Device Marking



- The above marking layout shows only marking contents and their approximate position, not actual font, size and exact position.

10. Soldering Pattern

Example of patterning design indicated as follows. In an actual design, please consider mounting density, the reliability of soldering, etc. and check whether performance is optimal.



11. Application Note

1. This device contains a crystal resonator, so please do not expose to excessive shock or vibration. The internal crystal resonator might be damaged in case that too much shock or vibration is produced mechanically. Be sure to check your machine condition in advance.
2. This device is made with C-MOS IC. Please take necessary precautions to prevent damage due to electrostatic discharge.
3. We recommend to use and store under room temperature and normal humidity to secure frequency accuracy and prevent moisture.
4. We will announce the discontinuance and switch to our successor before six months or more.
5. Recommendation reflow times are less than 3 times.

   When there was a soldering error, please do alteration with a soldering iron. In this case, the iron ahead is equal to or less than +350 ºC and asks within 5 s.

   In case that this device is reflow soldered on the back side of your circuit board, please carefully verify the device is properly secured to prevent coming detached from card.

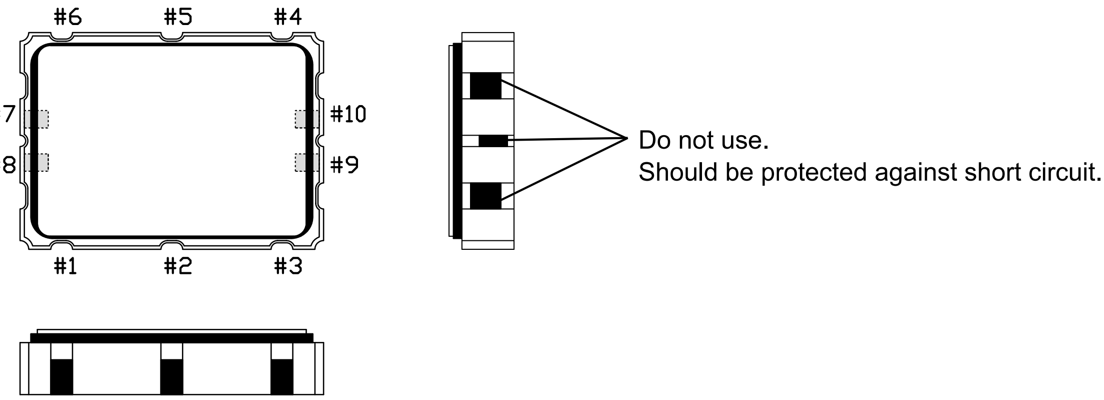
Soldering method

Soldering method	Good or No good
Reflow soldering (top side)	Good
Reflow soldering (back side)	Please carefully verify the device is properly secured to prevent coming detached from card.
Solder pot (static solder pot/flow solder pot)	No good
Iron soldering	Good

6. Ultrasonic cleaning can be used on this product, however, since the oscillator might be damaged under some conditions, please exercise caution in advance.
7. Protection against periodically mechanical vibration

   While there is any given shock or mechanical vibration periodically to crystal products, such as, a cooling fan, a piezo sounder, a piezo buzzer, and a speaker to crystal products, output frequency and amplitude can be changed. Especially the quality of telecommunication equipment could be affected by this phenomenon. Although Epson's crystal products are designed to minimize the effect of mechanical vibration, we recommend checking them in advance.
8. The metal part of the surface (metal cap) is connected to GND #3 pin. Please take necessary precautions to prevent short circuit to GND by contact with the metal cap.

9. Side leads as shown below are connected to IC internally. Therefore be careful for short or a fall of insulation resistance.



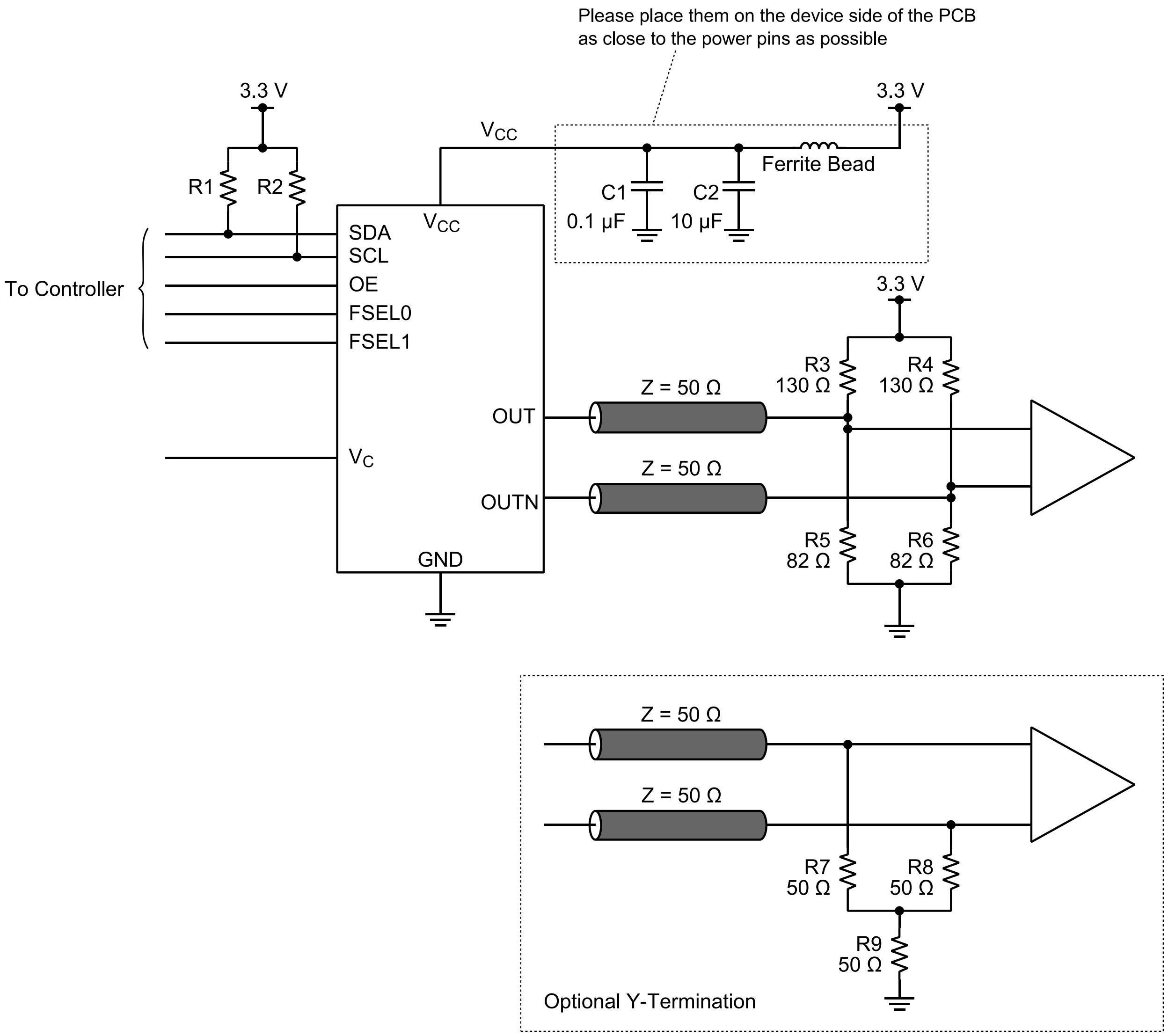
10. V_{CC} and GND pattern shall be as large as possible so that high frequency impedance shall be small.
11. Seiko Epson doesn't recommend to power on from intermediate electric voltage or extreme fast power on. Those powering conditions may cause no oscillation or abnormal oscillation.
12. Please design the output lines by characteristic impedance 50 Ω and try to make the output lines as short as possible. A long output line may cause irregular output. Other high level signal lines may cause incorrect operation, so please do not place high-level signal line close to this device.
13. If OE (Active High), SDA or SCL pin is not used, please connect them to V_{CC}. In order to suppress surge, resister may be used for OE pin.
14. If output pin is connected to the ground when supply voltage is applied to product, the internal elements can be destroyed. So please use the products that always have connection with load resistance.

■ Example of VG7050ECN schematic layout

This figure shows an example of this product’s application schematic.

As with any high speed analog circuitry, the power supply pins for VG7050ECN are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.

In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible. The component value of this filter is just an example, it may have to be adjusted.



Application Manual

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