DATASHEET

General Description

The YQ1D208D is a 2-GHz, 8-output differential high- performance clock fanout buffer.

The YQ1D208D clock buffer allocates either of the two selectable clock inputs (IN0 and IN1) across eight pairs of differential LVDS clock outputs, ensuring minimal skew in clock distribution. This device is capable of receiving two clock sources through an input multiplexer. The permissible inputs include LVDS, LVPECL, or LVCMOS. It supports a maximum clock frequency of up to 2 GHz.

The device is engineered to distribute high-frequency, low phase-noise clock and data signals. It functions with a core power supply of either 2.5V or 3.3V and supports an output operating supply of 2.5V or 3.3V.

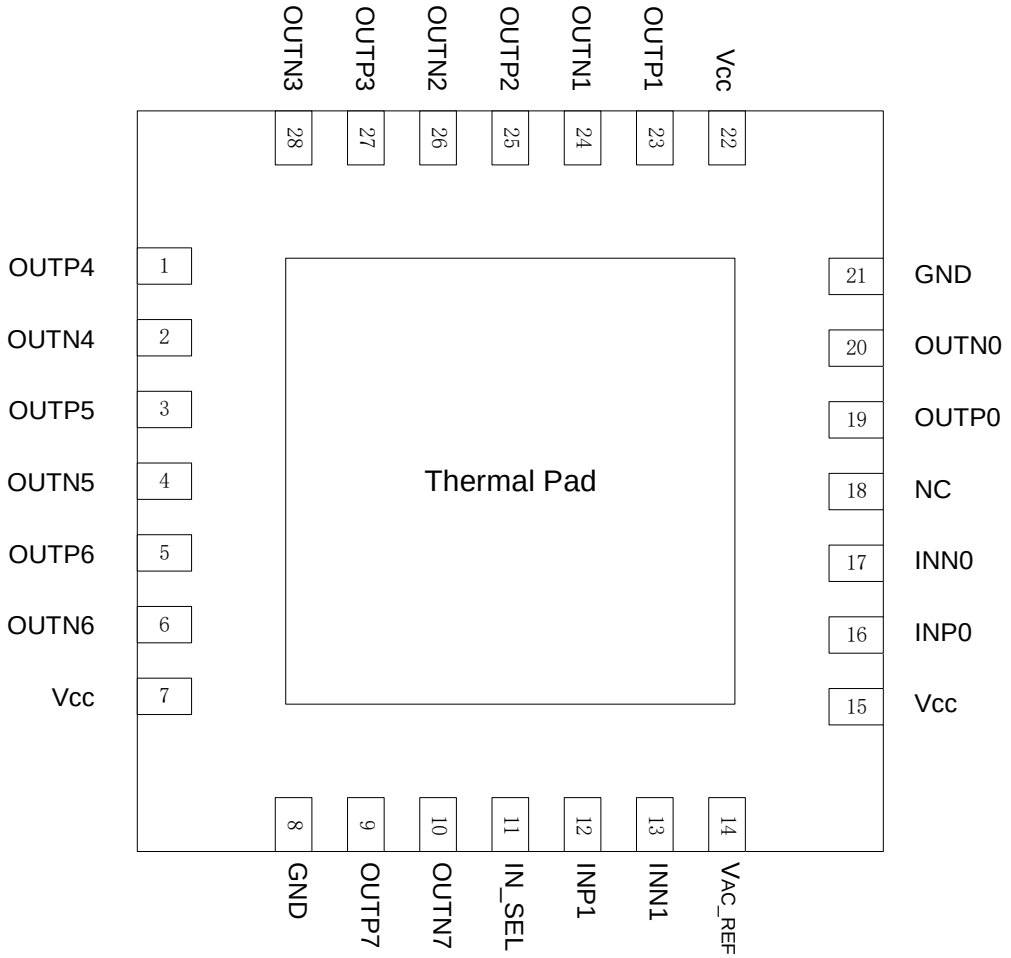
Features

- 2:8 Differential Buffer
- Universal inputs can accept LVPECL, LVDS, HCSL and LVCMOS
- Eight LVDS outputs
- Maximum output frequency – LVDS 2GHz
- Maximum propagation delay: 0.5ns(typical)
- Output skew: 50ps (Maximum)
- Part-to-part skew: 300ps (Maximum)
- Additive RMS phase jitter @ 156.25MHz: < 100 fs RMS (10kHz - 20MHz)
- Supply voltage mode VDD: 2.375V to 3.465V
- Industrial Temperature Range: -40°C to 85°C
- Available in 5*5 28-Pin QFN Package

Applications

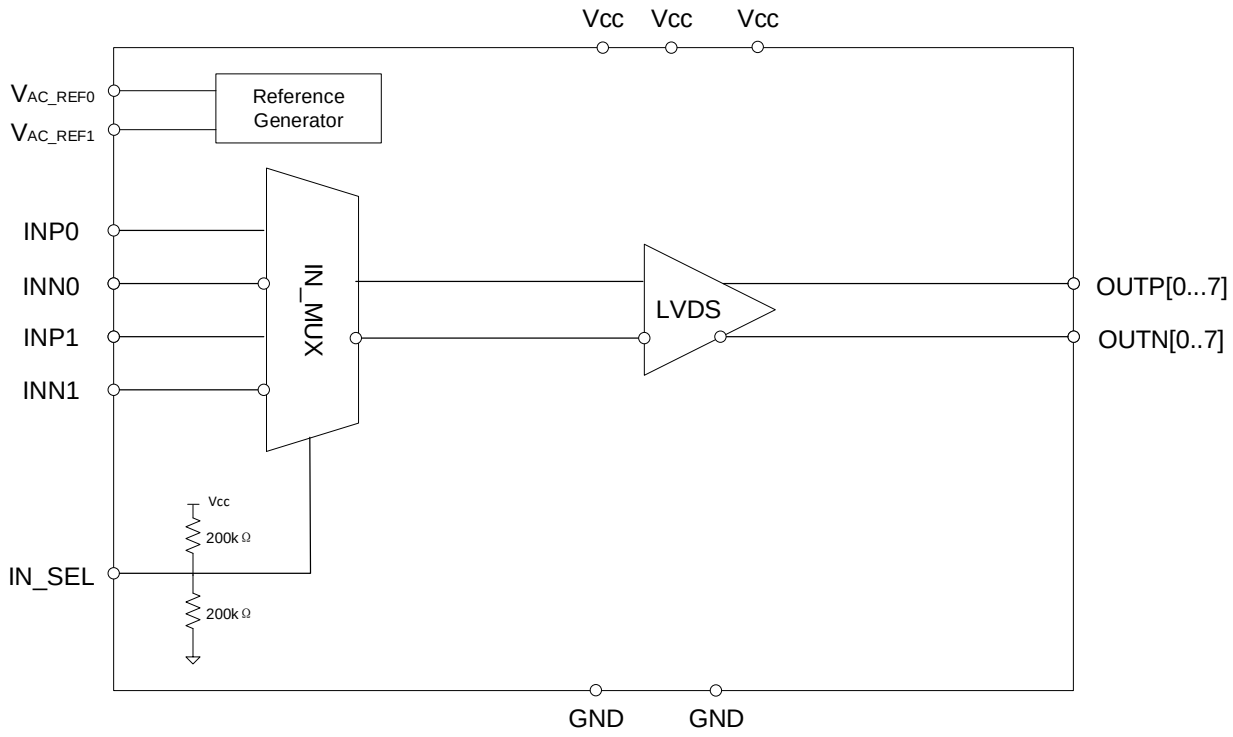
- Clock Distribution and Level Translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH, CPRI, High Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express (PCIe 3.0, 4.0)
- Remote Radio Units and Baseband Units
- Test and Measurement

Pin Configuration



5*5 28-pin QFN (Top View)

Block Diagram



Pin Descriptions

Number	Name	Type	Description
1	OUTP4	Output	Differential LVDS output pair number 4.
2	OUTN4	Output	Differential LVDS output pair number 4.
3	OUTP5	Output	Differential LVDS output pair number 5.
4	OUTN5	Output	Differential LVDS output pair number 5.
5	OUTP6	Output	Differential LVDS output pair number 6.
6	OUTN6	Output	Differential LVDS output pair number 6.
7	V_{CC}	Power	supply for the device.
8	GND	Ground	Device ground.
9	OUTP7	Output	Differential LVDS output pair number 7.
10	OUTN7	Output	Differential LVDS output pair number 7.
11	IN_SEL	Input	Input clock selection; selects input port differential input or single-ended input.
12	INP1	Input	Differential redundant input pair or single-ended input.
13	INN1	Input	Differential redundant input pair or single-ended input.
14	V_{AC_REF}	Output	NC
15	V_{CC}	Power	supply for the device.
16	INP0	Input	Differential redundant input pair or single-ended input.
17	INN0	Input	Differential redundant input pair or single-ended input.
18	NC	NC	NC
19	OUTP0	Output	Differential LVDS output pair number 0.
20	OUTN0	Output	Differential LVDS output pair number 0.

21	GND	Ground	Device ground.
22	V_{CC}	Power	supply for the device.
23	OUTP1	Output	Differential LVDS output pair number 1.
24	OUTN1	Output	Differential LVDS output pair number 1.
25	OUTP2	Output	Differential LVDS output pair number 2.
26	OUTN2	Output	Differential LVDS output pair number 2.
27	OUTP3	Output	Differential LVDS output pair number 3.
28	OUTN3	Output	Differential LVDS output pair number 3.

Functions Table

Table 1: Input Selection

IN_SEL[1:0]	Selected Input
0	INP0, INN0
1	INP1, INN1

Absolute Maximum Ratings

Stresses greater than these listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Item	Rating
Supply voltage, Vcc	-0.5 to 4.6V
Input Voltage, V_{IN}	-0.5V to Vcc+ 0.5V
Junction Temperature	125°C
Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2023	±5000	V
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±2000	

Latch Up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78F.02-2023	±450	mA
	V-test, JEDEC STD JESD78F.02-2023	4.95	V

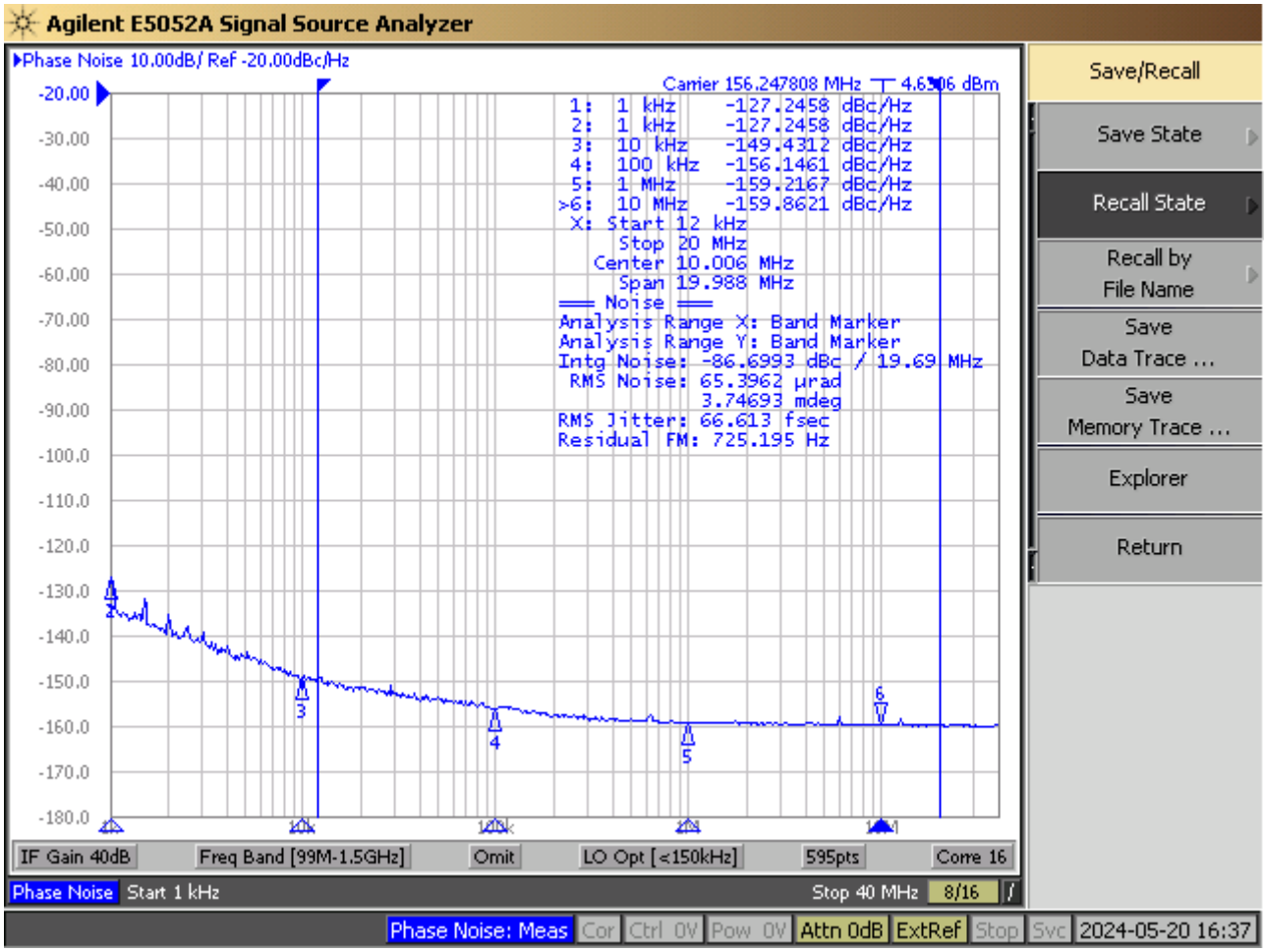
Power Supply Characteristics Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	℃
T_J	Junction temperature			125	℃
Vcc	Power supply for Crystal core and input blocks	2.375		3.465	V

Electrical Characteristics

Additive Phase Jitter

Phase noise, also known as dBc Phase Noise, measures the cleanliness of a frequency band around a central frequency compared to the strength of that central frequency itself. This measurement is typically shown on a phase noise plot, which is commonly used in many technical applications. Phase noise represents the noise power in a 1Hz bandwidth at a certain distance from the central or fundamental frequency, relative to the power of the central frequency. This relationship is expressed in decibels (dBm) or as a ratio of power between the 1Hz band and the fundamental frequency. When a specific offset is defined, this measurement is referred to as a dBc value, indicating dBm at that particular offset. By analyzing jitter through the frequency domain, we gain a clearer insight into its impact on an application across the entire duration of the signal. From a phase noise plot, it is possible to mathematically predict an expected bit error rate.



POWER CONSUMPTION

Parameter		Test Conditions	Min	Typ	Max	Unit
Icc	Typical power consumption	Differential load 100Ω, operating frequency 156.25MHz.		145		mA

CMOS Control Inputs

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		1.6		VDD	V
V_{IL}	Low-Level Input Voltage		GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = VDD, Internal pulldown resistor			60	uA
I_{IL}	Low-Level Input Current	V_{IL} = 0V, Internal pulldown resistor		0.1		uA

Clock Inputs (INN0/INP0, INN1/INP1)

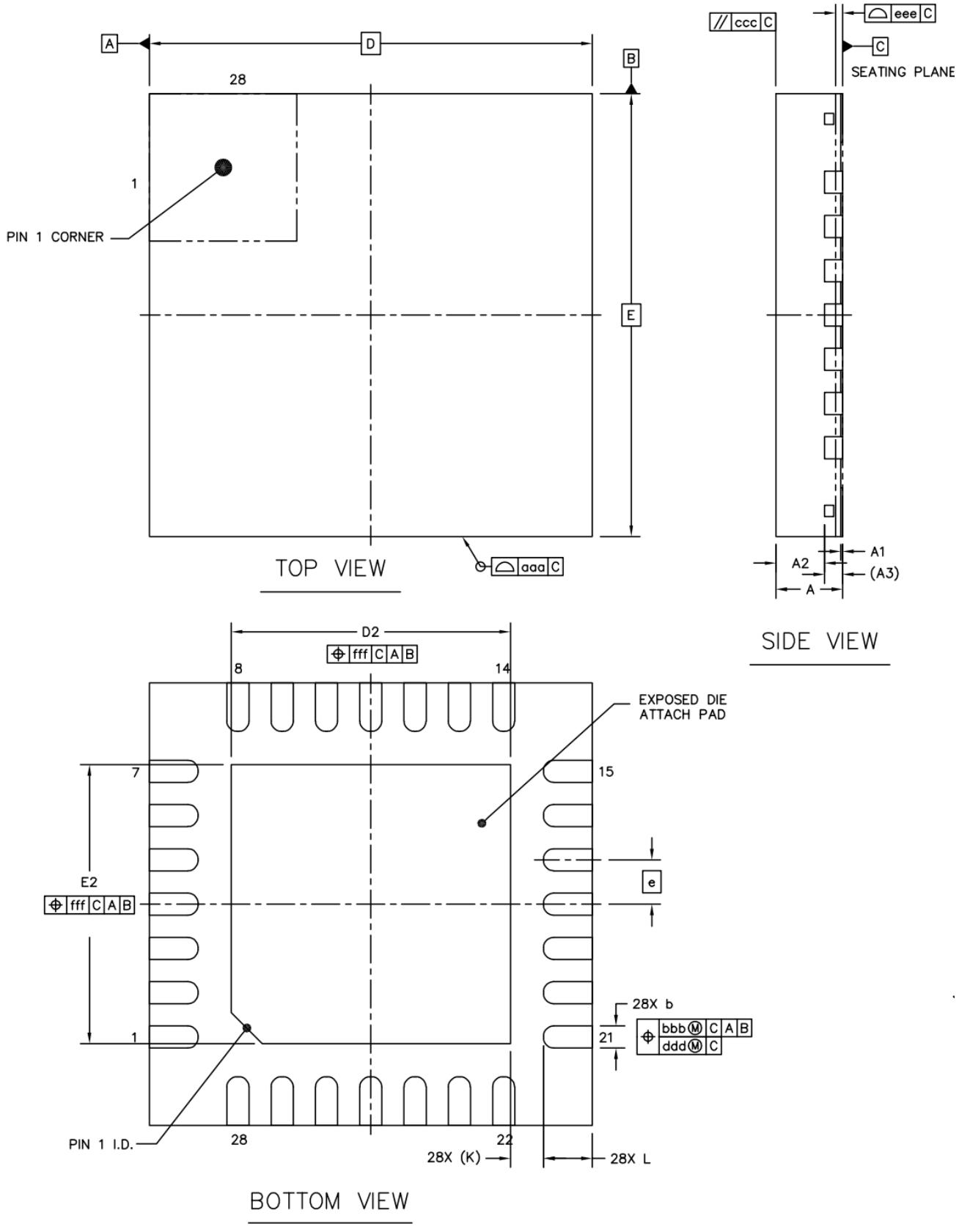
Parameter		Test Conditions	Min	Typ	Max	Unit
F_{CLKin}	Input Frequency Range		DC		2000	MHz
V_{IHD}	Differential Input High Voltage	Driven differentially			Vcc	V
V_{ILD}	Differential Input Low Voltage		GND			V
V_{ID}	Differential Input Voltage Swing		0.1		1.5	V
V_{CMD}	Differential Input Common Voltage	V_{ID} = 200mV	0.25		Vcc-1.2	V
V_{IH}	Singel-ended Input High Voltage	INNx/INPx driven single-ended (AC or DC coupled)			Vcc	V
V_{IL}	Singel-ended Input Low Voltage		GND			V
V_{I_SE}	Singel-ended Input Voltage Swing		0.3		2.2	V_{PP}
V_{CM}	Singel-ended Input Common Voltage		0.25		Vcc -1.2	V

LVDS OUTPUTS

Parameter		Test Conditions		Min	Typ	Max	Unit
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing	V_{OD} ≥ 250 mV, R_L = 100 Ω differential			1.45		GHz
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing	V_{OD} ≥ 200 mV, R_L = 100 Ω differential			2		GHz
$Jitter_{ADD}$	Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz	VDDO = 3.3 V, R_L = 100 Ω differential	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns		55		fs

Noise Floor	Noise Floor $f_{OFFSET} \geqslant$ 10MHz	VDDO = 3.3 V, R_L = 100 Ω differential	CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns	-160			dBc/Hz
DUTY	Duty Cycle	50% input clock duty cycle		45%		55%	
V_{OD}	Output Voltage Swing	T_A = 25 °C, DC Measurement, R_L = 100 Ω differential		250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States			-35		35	mV
V_{OS}	Output Offset Voltage			1.1	1.25	1.35	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States			-30		30	mV
t_R	Output Rise Time 20% to 80%	Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R_L = 100 Ω differential, $C_L \leq$ 5 pF			200	400	ps
t_F	Output Fall Time 80% to 20%				200	400	ps
t_{PD}	Propagation delay	VIN, DIFF, PP = 0.3 V			0.5	1.5	ns
$t_{SK,pp}$	Part-to-part skew					300	ps
$t_{SK,O}$	Output skew				10	50	ps
$t_{SK,P}$	Pulse skew	50% duty cycle input,crossingpoint-to-crossing-point distortion		-50		50	ps,RMS

Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.05	3.15	3.25
	Y	E2	3.05	3.15	3.25
LEAD LENGTH		L	0.45	0.55	0.65
LEAD TIP TO EXPOSED PAD EDGE		K		0.375 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Revision History

No	Date	Description
V1.0	2024.05.17	Initial release