VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO)
OUTPUT : LV-PECL, LVDS

VG3225 / 5032 / 7050EFN
VG3225 / 5032 / 7050VFN

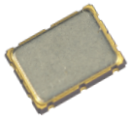
Pb Free
RoHS Compliant

Product Number
VG3225EFN X1G005361xxxx00
VG5032EFN X1G005471xxxx00
VG7050EFN X1G005491xxxx00
VG3225VFN X1G005461xxxx00
VG5032VFN X1G005481xxxx00
VG7050VFN X1G005501xxxx00

- Frequency range : 25 MHz to 500 MHz (VG3225EFN / VG3225VFN)
  25 MHz to 250 MHz (All other)
- Supply voltage : 3.3 V Typ.
- Output : LV-PECL or LVDS
- Function : Output enable (OE)
- Absolute pull range : ±10 × 10^{-6} Min. / ±20 × 10^{-6} Min. / ±50 × 10^{-6} Min
- Operating temperature : -40 °C to +85 °C / -40 °C to +105 °C


VG3225EFN
VG3225VFN
(3.2 × 2.5 × 1.05 mm)


VG5032EFN
VG5032VFN
(5.0 × 3.2 × 1.3 mm)


VG7050EFN
VG7050VFN
(7.0 × 5.0 × 1.5 mm)

Specifications (characteristics)

Item	Symbol	Specifications		Conditions / Remarks	
		LV-PECL	LVDS		
		VG3225EFN / VG5032EFN / VG7050EFN	VG3225VFN / VG5032VFN / VG7050VFN		
Output frequency range	fo	25 MHz to 500 MHz		VG3225EFN / VG3225VFN	Please contact us for available frequencies.
		25 MHz to 250 MHz		All other	
Supply voltage	V_{CC}	C: 3.3 V ± 0.165 V			
Control voltage	Vc	1.65 V ±1.65 V			
Storage temperature	T_stg	-55 °C to +125 °C			
Operating temperature	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C			
Frequency tolerance	f_tol	J: ±50 × 10^{-6} Max.		Includes initial frequency tolerance, temperature variation, supply voltage change and 10 years aging (+25 °C) at Vc = 1.65 V	
Absolute Pull range *1	APR	B: ±50 × 10^{-6} Min.		25 MHz ≤ fo ≤ 42.5 MHz, 50 MHz ≤ fo ≤ 85 MHz, 100 MHz ≤ fo ≤ 170 MHz	
		M: ±20 × 10^{-6} Min.		25 MHz ≤ fo ≤ 250 MHz	
		S: ±10 × 10^{-6} Min.		25 MHz ≤ fo ≤ 250 MHz	
				250 MHz < fo ≤ 500 MHz, T_use: G (-40 °C to +85 °C)	
Current consumption	I_{CC}	60 mA Max.	25 mA Max.	OE = V_{CC}, L_ECL = 50 Ω or L_LVDS = 100 Ω	
Disable current	I_dis	25 mA Max.	15 mA Max.	OE = GND	
Input impedance	Zin	10 MΩ Min.		DC level	
Frequency change polarity	-	Positive slope		V_C = 0 V to 3.3 V	
Symmetry	SYM	45 % to 55 %		At output crossing point	
Output voltage (LV-PECL)	V_{OH}	V_{CC} - 1.1 V Min.	–	DC characteristics	
	V_{OL}	V_{CC} - 1.5 V Max.	–		
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	Differential output voltage, V_{OD1}, V_{OD2}	DC characteristics
	V_{OS}	–	1.15 V to 1.35 V	Offset voltage, V_{OS1}, V_{OS2}	
ECL load condition	L_ECL	50 Ω	–	Terminated to V_{CC} - 2.0 V	
LVDS load condition	L_LVDS	–	100 Ω	Connected between OUT to $\overline{OUT}$	
Input voltage	V_{IH}	70 % V_{CC} Min.		OE terminal	
	V_{IL}	30 % V_{CC} Max.			
Rise/Fall times	tr / tf	0.5 ns Max..	0.3 ns Max.	LV-PECL: Between 20 % and 80 % of (V_{OH} - V_{OL}) LVDS: Between 20 % and 80 % of Differential Output peak to peak voltage	
Startup time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s	
Phase Jitter	t_{PJ}	120 fs Max.	160 fs Max.	fo = 122.88 MHz	Offset Frequency 12 kHz to 20 MHz
		80 fs Max.	80 fs Max.	fo = 245.76 MHz	
		70 fs Max.	80 fs Max.	fo = 491.52 MHz	

*1 Absolute pull range = Frequency control range- Frequency tolerance
* Please keep Vc pin open or ground while powering up V_{CC}.

Product Name (Standard form)
VG3225 EFN 122.880000MHz C J G H B A
① ② ③ ④⑤⑥⑦⑧⑨
①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency
④Supply voltage (C: 3.3 V Typ.) ⑤Frequency tolerance ⑥Operating temperature
⑦OE Function ⑧Absolute Pull Range ⑨Output Standby Type (A: High-Z)

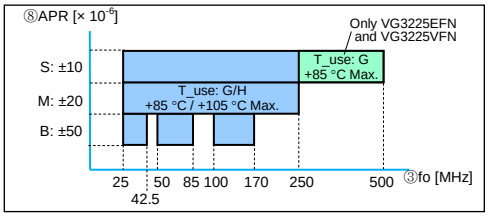
⑤Frequency tolerance	
J	±50 × 10^{-6}

⑥Operating temperature	
G	-40 to +85 °C
H	-40 to +105 °C

⑦OE Function	
H	Active High

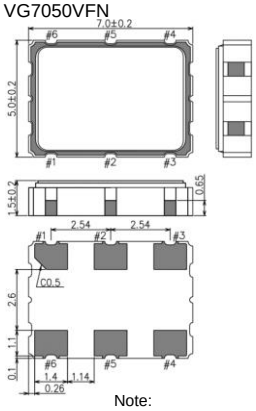
⑧Absolute Pull Range	
B	±50 × 10^{-6}
M	±20 × 10^{-6}
S	±10 × 10^{-6}

Figure 1 Available combination of ③Output frequency (fo) and ⑧Absolute Pull Range (APR)

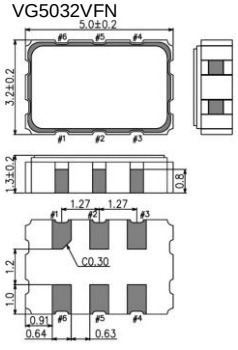


External dimensions (Unit:mm)

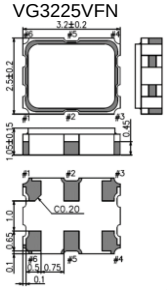
VG7050EFN
VG7050VFN



VG5032EFN
VG5032VFN



VG3225EFN
VG3225VFN

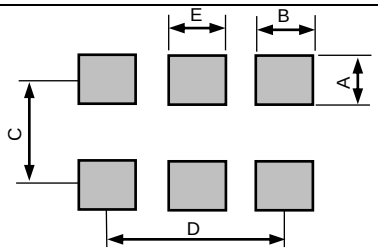


Note:
OE pin = HIGH or "Open": Specified frequency output.
OE pin = LOW: Output is high impedance

Pin map

Pin	Connection
1	Vc
2	OE
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Footprint (Recommended) (Unit:mm)



	VG3225EFN VG3225VFN	VG5032EFN VG5032VFN	VG7050EFN VG7050VFN
A	1.05	1.60	2.00
B	0.92	0.89	1.80
C	1.85	2.60	4.20
D	2.58	2.54	5.08
E	0.80	0.89	1.80

In order to achieve optimum jitter performance, it is recommended that 0.1 µF and 10 µF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.

PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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	►Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	►Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
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